

Deep dry etching process development for InP-based photonic crystals

R. van der Heijden, E. van der Drift*, E.J. Geluk, R.W. van der Heijden, F. Karouta, P.A.M. Nouwens, Y.S. Oei, T. de Vries, H.W.M. Salemink

COBRA Inter-University Research Institute, Eindhoven University of Technology,
PO Box 513, NL 5600 MB Eindhoven, The Netherlands.

* Delft Institute for Microelectronics and Submicron Technology,
Delft University of Technology, P.O. Box 5053, 2600 GB Delft, The Netherlands

A double layer mask strategy involving e-beam lithography, Reactive Ion Etching (RIE) of a Si_xN_y-mask and deep Inductively Coupled Plasma (ICP) InP-etching, has been applied to fabricate 2D photonic crystals in InP. Key parameters for the RIE-process are RIE-lag and lateral etching of the PMMA-mask. Important issues for the ICP-process are floor roughness and sidewall-angle and -roughness of the holes. Significant difference between n-type and semi-insulating InP after ICP etching has been observed.

Introduction

Two-dimensional (2D) photonic crystals in the InP-material system are of great importance, since they can be integrated with planar optical circuits based on standard InP-InGaAsP ridge waveguides with available lithographic techniques. The fabrication of these 2D photonic crystals in InP-InGaAsP waveguide structures forms a major technological challenge however, as ~250 nm diameter holes must be etched several microns deep with vertical sidewalls and nanometer tolerances on sidewall-roughness.

The objective of the present work is the fabrication of high aspect ratio hole-type 2D photonic crystals in an InP-InGaAsP waveguide structure using a double layer mask strategy [1-4]. This involves Electron-Beam Lithography (EBL), pattern transfer to a Si_xN_y-mask layer with Reactive Ion Etching (RIE) and deep Inductively Coupled Plasma (ICP) InP-etching. To have a sufficiently large photonic band gap centered around the long-haul telecommunication free space wavelength of 1550 nm, the crystal must have a lattice constant a of about 400 nm and the holes must have a diameter d of about 250 nm. In order to minimize non-intrinsic losses, the holes forming the photonic crystal must fully overlap with the mode profile of the optical signal. Therefore it is required, that the holes are etched 2.5 μm deep into the InP-InGaAsP waveguide structure with straight sidewalls, thus having an aspect ratio of 10.

Dielectric mask deposition

A Si_xN_y-layer with a thickness of 400 nm was deposited on InP by Plasma Enhanced Chemical Vapor Deposition (PECVD). The thickness of this layer is chosen such as to enable the final deep etching step in InP, taking into account the InP/Si_xN_y etch selectivity and allowing for an etch lag in deep holes.

Electron-Beam Lithography (EBL)

Two-dimensional triangular photonic crystal lattices were written into an 1100 nm thick PMMA 950 K e-beam resist layer with a 100 kV Leica EBL system. The PMMA-layer thickness is chosen such as to enable the pattern transfer to the Si_xN_y-layer in the RIE-process, accounting for the Si_xN_y/PMMA etch selectivity and allowing for an etch lag in small-diameter holes. After development, the samples were cleaved through the photonic crystal pattern and the cross-section of the holes was characterized by scanning electron microscopy (SEM). A SEM picture of the resulting holes in the PMMA-layer for a lattice which was designed to have $a = 400$ nm

and $d = 160$ nm, is displayed in figure 1. Notice the vertical sidewalls of the photonic crystal holes. The diameter of the holes was measured from figure 1 to be 200 nm, so significantly larger than the designed 160 nm. This effect could be due to lateral etching inside the PMMA-holes during development, induced by parasitic exposure due to backscattered electrons.

Reactive Ion Etching (RIE) transfer to the Si_xN_y -mask

After EBL, PMMA patterns were transferred into the Si_xN_y -layer using two different CHF_3/O_2 -based RIE-processes in different reactors. The relevant parameters of this process are detailed in table 1. The given etch rates and selectivity's are values for large area etches.

Table 1: Parameters of the used RIE-processes

Process number	Pressure (Pa)	CHF_3 -flow (sccm)	O_2 -flow (sccm)	RF-power (W)	Si_xN_y -etch rate (nm/min)	$\text{Si}_x\text{N}_y/\text{PMMA}$ -selectivity
1	0.6	50	2.5	50	24	0.7
2	6.6	50	5	100	70	1.3

Process 1 was used to transfer the pattern shown in figure 1 to the Si_xN_y -layer. A SEM-picture of the cross-section of the resulting holes after 21 minutes of etching is displayed in figure 2. It is visible in this figure, that the holes in the Si_xN_y -mask are fully opened after this procedure. The Si_xN_y -etch rate for these holes is thus at most a factor of 1.3 smaller than the large area etch rate for process 1. The dependence of etch rate on structure-dimension is a known effect for RIE-processes and is often referred to as RIE-lag [5]. The sloped sidewalls of the holes are a distinct feature in the etch-result of figure 2. This feature is attributed to lateral etching of the PMMA-mask during the RIE-process. From a comparison of the width of the holes in the PMMA-mask (figure 1) with the top-width of the holes in the Si_xN_y -mask (figure 2) it is calculated that this lateral etch rate is 1 nm/min. Photonic crystal patterns with different dimensions are etched with various etch-times using process 2, to determine both the RIE-lag and the lateral PMMA-etch rate of this process. SEM-measurements of the etch-depth of the holes in the Si_xN_y -layer after 4 minutes of etching have been performed for various hole-diameters. The hole-diameters were also measured from SEM-pictures. The results are displayed in figure 3. From this figure it is determined, that the Si_xN_y -etch rate for ~ 200 nm holes is a factor of 2 smaller than the large area etch rate for process 2. It is believed, that the difference in RIE-lag between process 1 and process 2 is mainly due to the difference in process-pressure [5]. The lateral etch rate of process 2 is determined by SEM-measurements of the top hole-width in the Si_xN_y -layer as a function of etch-time for different photonic crystal patterns. The results are displayed in figure 4.

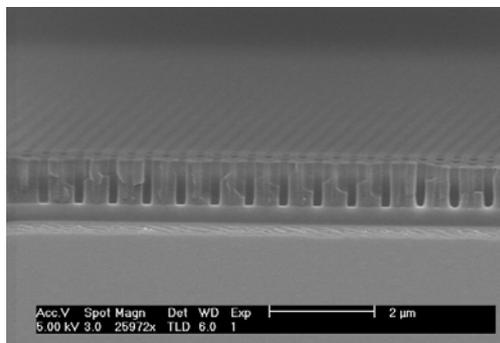


Figure 1: SEM picture of the cross-section of the photonic crystal lattice in the PMMA layer after EBL. The 400 nm thick Si_xN_y -layer is visible below the holes.

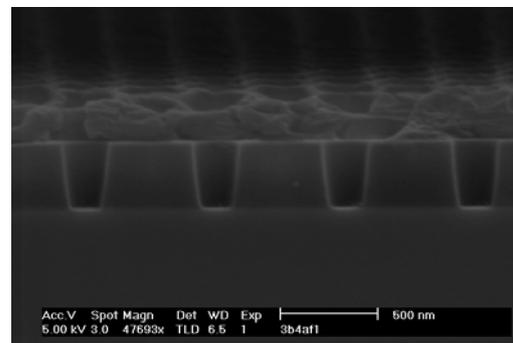


Figure 2: SEM picture of the cross-section of the photonic crystal lattice in the Si_xN_y -layer after process 1. Remaining PMMA is visible on top of the Si_xN_y -mask.

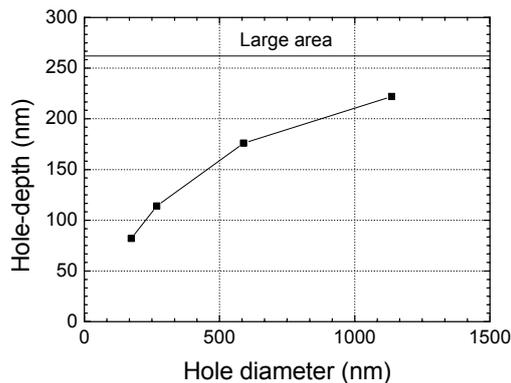


Figure 3: Measured hole-depth in Si_xN_y after 4 minutes of RIE (process 2) as a function of hole-diameter. The large area etch-depth of 260 nm is displayed as a horizontal line.

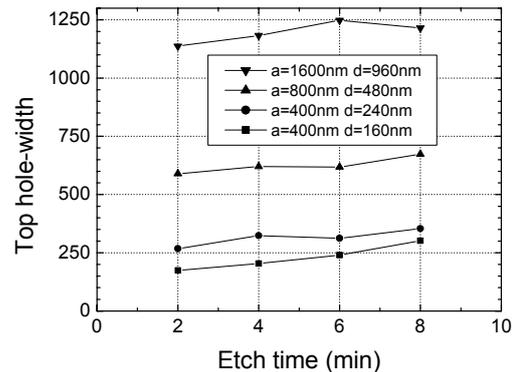


Figure 4: Measured top hole-width in Si_xN_y as a function of RIE-time (process 2) for different photonic crystal patterns written in the PMMA.

Note that the hole-diameters that are specified in figure 4 are the designed values. The real values after EBL are significantly larger, which was discussed earlier for the ($a = 400$ nm, $d = 160$ nm) case. From figure 4, the lateral PMMA-etch rate of process 2 is determined to be 8-12 nm/min. The ratio of the lateral PMMA-etch rate to the vertical Si_xN_y -etch rate is thus about 0.15 for process 2, which is a factor of 3 larger than for process 1. The lateral PMMA-etch rate is most probably related to the O_2 -partial pressure in the plasma during etching, which is higher in process 2. It is crucial that the photonic crystal holes in the Si_xN_y -mask exhibit vertical sidewalls to be able to etch holes with vertical sidewalls in InP. Further reduction of the (lateral PMMA-etch rate to vertical Si_xN_y -etch rate)-ratio is thus important for process 2 but even for process 1.

Inductively Coupled Plasma (ICP) etching of InP

In the final fabrication step photonic crystal patterns are deeply etched into the InP with a $\text{Cl}_2/\text{H}_2/\text{CH}_4$ -based ICP-process, using the Si_xN_y -layer as etch-mask. These experiments were carried out in an Oxford Plasmalab ICP-reactor. The relevant parameters of the process were as follows: pressure = 4 mTorr (0.5 Pa), Cl_2 -flow = 7 sccm, H_2 -flow = 8 sccm, CH_4 -flow = 5.5 sccm, ICP-power = 1000 W, RF-power = 100 W. A large area InP etch rate of 1.2 $\mu\text{m}/\text{min}$ with an InP/ Si_xN_y selectivity of 10 was obtained with this process. Only samples that were treated with RIE-process 2 were etched with the ICP-process so far. The ~ 200 nm diameter holes in the Si_xN_y -mask were not fully opened for these samples. It is estimated that, for these holes, the first minute of a 2-minute ICP-etch was necessary to etch through the mask. The resulting holes in the InP after the ICP-process therefore had a conical shape and a depth of 0.8 μm . The photonic crystal holes of the ($a = 1600$ nm, $d = 960$ nm) lattice were also etched with RIE-process 2 and were fully opened. SEM-pictures of these holes after the ICP-process are displayed in figure 5. The depth of the holes in figure 5 was measured to be 2.1 μm and the etch rate for these holes was thus 1.1 $\mu\text{m}/\text{min}$, close to the large area etch rate. The result of figure 5 was obtained with Sn-doped n-type InP-substrates. Similar experiments were performed for Fe-doped semi-insulating InP-substrates. A SEM-picture of the ($a = 1600$ nm, $d = 960$ nm)-holes after 3 minutes of ICP-etching is shown in figure 6. The etch rate for the holes in the semi-insulating InP-sample was determined from figure 6 to be 0.7 $\mu\text{m}/\text{min}$, so significantly lower than for the n-type sample. A striking difference between the n-type and semi-insulating sample occurs at the floor of the holes. The floor of the hole is completely smooth for the n-type sample and

exhibits a grass-type roughness for the semi-insulating sample. Grass-type floor roughness is a commonly known feature for InP-samples that are dry-etched with Cl-based chemistry and is usually assigned to InCl_x -micro-masking [6], [7]. Another important difference is that the holes of the semi-insulating sample exhibit more vertical sidewalls than the holes of the n-type sample. The sidewalls of the holes appear to be rough for both the n-type and the semi-insulating samples. It seems that the mechanism causing wall roughness is not correlated with the mechanism causing floor roughness. The cause of the observed difference in floor roughness and verticality between semi-insulating and n-type samples is not known. As the temperature of the sample is not explicitly controlled in the described ICP-process, a temperature effect is possible. However, electric-field effects by local charging might also play a role. Finding the cause of the observed difference could lead to a better understanding of the ICP-process and could thus contribute to improvement of the final etching result.

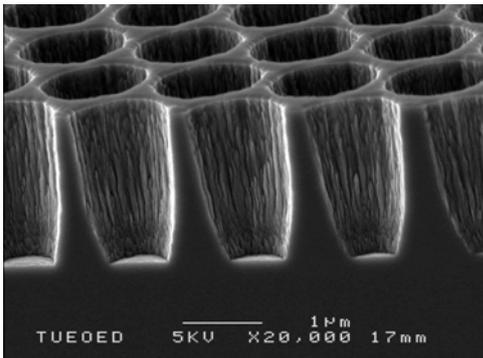


Figure 5: Cross-section of the ($a = 1600$ nm, $d = 1000$ nm) photonic crystal lattice after 2 minutes of ICP-etching for Sn-doped n-type InP substrate.

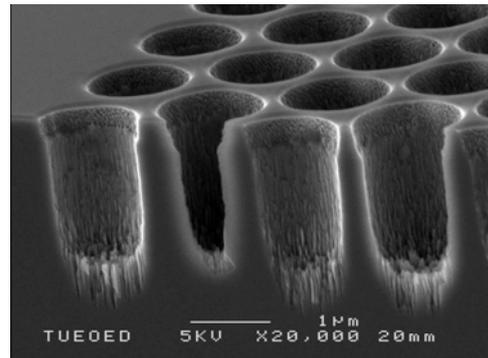


Figure 6: Cross-section of the ($a = 1600$ nm, $d = 1000$ nm) photonic crystal lattice after 3 minutes of ICP-etching for Fe-doped semi-insulating InP substrate.

References

- [1] T. Happ, A. Markard, M. Kamp, A. Forchel, S. Anand, J.-L. Gentner, and N. Bouadma, *J. Vac. Sci. Technol. B* **19**, 2775 (2001).
- [2] R. Ferrini, D. Leuenberger, M. Mulot, Min Qiu, R. Moosburger, M. Kamp, A. Forchel, S. Anand, and R. Houdre, *IEEE J. Quant. Elec.* **38**, 786 (2002).
- [3] A. Djoudi, L. Le Gouezigou, S. Hubert, S. Sainson, C. Moussant, J-P. Chandouineau, F. Pommereau and G-H. Duan, *Proc. 14th Indium Phosphide and Related Materials Conf.*, Stockholm, Sweden, May 2002.
- [4] P. Strasser, R. Wüest, F. Robin, D. Erni and H. Jäckel, *Proc. 27th Workshop Compound Semicond. Dev. & Integrated Circuits*, FÜRIGEN, Switzerland, May 2003
- [5] R. Gottscho, C. W. Jurgensen and D. J. Vitkavage, *J. Vac. Sci. Tech. B* **10**, 2133 (1992)
- [6] B. Lamontagne, J. Stapledon, P. Chow-Chong, M. Buchanan, J. Fraser, J. Phillips and M. Davies *J. Electrochem. Soc.* **146**, 1918 (1999)
- [7] M. Vernon, T. R. Hayes and V. M. Donnelly *J. Vac. Sci. Technol. A* **10**, 3499 (1992)