Monolithic transimpedance amplifier design for large photodiode capacitance and wide temperature range

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In this paper we present a study on the front-end of an optical receiver operating at 850 nm with a large integrated Si photodiode. The large photodiode implies a large capacitance. Combined with the low responsivity at 850nm this makes the design of a receiver with high bandwidth and high sensitivity challenging, especially when the junction temperature range from -40°C till 140°C. We compare different front-end topologies and suggest a method to compensate for the variations over temperature of the bandwidth. It is shown that a common-emitter front-end provides best sensitivity as long as the required bandwidth can be achieved.

Introduction

Low cost high sensitivity optical receivers (Rx) operating at a wavelength of 850 nm find widespread applications, such as in the automotive market. To reduce costs, the photodetector is preferably integrated together with the Si electronics. To relax mechanical tolerances, a large-area photodiode (PD) is preferred. Unfortunately, the responsivity of Si at 850 nm is low (about 0.2 till 0.4 A/W). Combined with the large capacitance of a large PD, this makes the design of a sensitive Rx challenging. On top of this, for automotive applications a wide temperature range is required. This paper addresses the design of a sensitive 150-Mbit/s transimpedance amplifier (TIA) that can operate over a wide temperature range, integrated together with a large PD in a 0.6 µm BiCMOS technology.

The front-end topology

The sensitivity of an optical Rx is limited by both the input-referred noise and by electrical crosstalk. An important consideration when using a PD integrated on the same die as the Rx electronics is possible crosstalk via the substrate. Indeed, switching noise induced by for example the output stage of the Rx is coupled to the input of the preamplifier through the substrate and via the PD capacitance. To limit the sensitivity degradation of the Rx by such crosstalk, a fully differential structure using a dummy PD is the preferred choice for a sensitive Rx, see Fig. 1 [1]. The dummy PD is shielded from any incoming light. Hence, the optical power impinging upon the actual PD is converted into a differential current and amplified by the differential TIA. Any crosstalk from the substrate is converted into a common-mode current and rejected by the TIA.

To achieve a high sensitivity, the input-referred noise of the TIA must be minimal. The input-referred noise consists of the thermal noise from the feedback resistor R_F (see Fig. 1) and the noise stemming from the transistors and resistors in the amplifier itself. To minimize the thermal noise of the feedback resistor R_F, this resistance should be chosen

as high as possible. This is limited by the fact that the 3dB bandwidth f_{3dB} of a TIA can be approximated as (assuming the dominant pole of the TIA is located at its input):

$$f_{3dB} = \frac{1}{2\pi} \frac{A_{V0}}{C_T R_F} \tag{1}$$

with A_{V0} the open-loop gain of the TIA, C_T the total capacitance at the input of the TIA and R_F the resistance value of the feedback resistor. Ideally, f_{3dB} should be around 100 MHz given the bit-rate of 150-Mb/s and the non-return-to-zero modulation format. To maintain the bandwidth despite increasing R_F, the open-loop gain A_{V0} should be increased proportionally. Ultimately, this is limited by stability concerns.

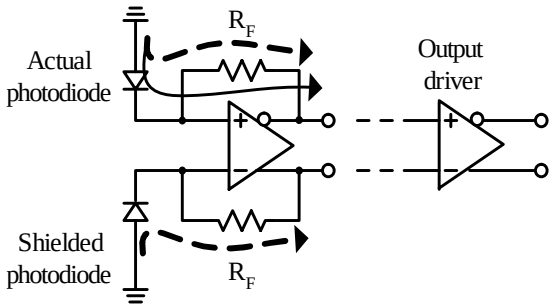

Figure 1 – Fully differential transimpedance amplifier using a shielded photodiode. Dashed lines indicates currents caused by substrate crosstalk, the solid line is the signal current.

Careful attention should be paid to the topology of the first stage of the TIA to minimize its input-referred noise. One can choose between CE/CS (common-emitter/common-source), CB/CG (common-base/common-gate) or CC/CD (common-collector/common-drain) topologies. CB/CG topologies offer the advantage of decoupling the relationship (1) between f_{3dB} and the PD capacitance [2]. Such topologies are therefore used if the PD capacitance limits the achievable bandwidth. The same is true for CC/CD topologies, although to a lesser extent. Unfortunately, the current gain of a CB/CG is unity, therefore the current noise from any subsequent stage is reflected back to the input of the TIA. Reciprocally, the same is true for the CC/CD topologies, as now the voltage gain is unity. As a CE/CS topology offers both voltage and current gain, the noise from subsequent stages can be neglected. Therefore, as long as the required bandwidth can be achieved, the CE/CS topology is the best choice for achieving high sensitivity.

One now still needs to make a choice between either a CE or a CS topology for the first stage. It is known that for the bit-rate under consideration, the use of a MOSFET transistor in the first stage of a TIA offers best sensitivity. The reason is that for an optimized (i.e. the feedback resistance is sufficiently high such that its thermal noise can be neglected) CE-TIA the dominant noise source is base current shot noise. A CS-TIA does not exhibit shot noise due to such currents. However, this comes at the cost of high power consumption. Indeed, due to the low g_m/C_{gs} of a MOS transistor compared to the bipolar transistor, large bias currents are needed to ensure sufficient bandwidth. Simulations show that for the used technology a CS TIA can exhibit a sensitivity of -

27.7 dBm at a current consumption of 17 mA (for a responsivity of 0.3 A/W and an extinction ratio of 6 dB). A CE TIA exhibits a sensitivity of -27.5 dBm at a current consumption of 3.6 mA. Therefore, a CE stage was used as first stage in the TIA.

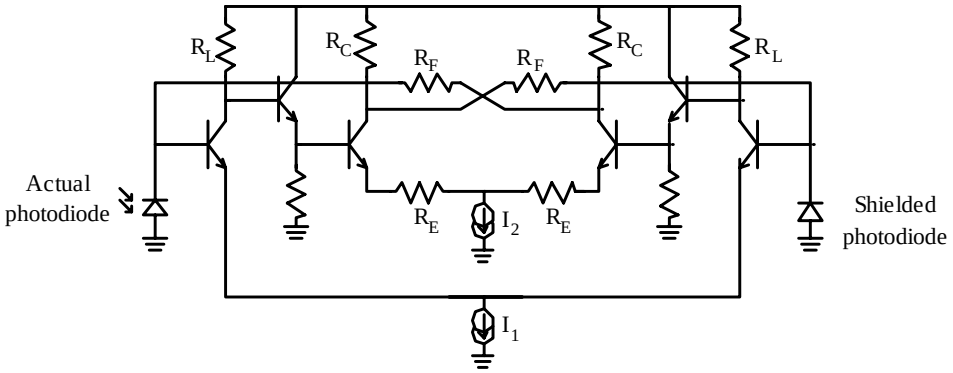

Figure 2 – Topology of the fully differential transimpedance amplifier.

The final topology of the differential TIA is shown on Fig. 2. The input CE stage is followed by an emitter-follower, to provide level-shifting and buffering. A second gain stage is inserted to increase the open-loop gain of the TIA, which allows increasing R_F while maintaining a bandwidth of about 100 MHz.

DC-biasing and temperature compensation

When designing the TIA, two points should be taken into account. First, the input common voltage should be as high as possible. Indeed, this reduces the PD capacitance and increases its responsivity, which helps to improve the sensitivity of the Rx. This common-mode voltage is determined by the value of R_C and the tail current of the second gain stage shown on Fig. 2. Secondly, the tail current of the first differential pair must be designed with a controlled temperature coefficient to ensure a bandwidth that is constant with temperature. Indeed, especially the tail current of the first differential pair is important, as the 3-dB bandwidth of the TIA is given as:

$$f_{3\,dB} \cong \frac{1}{2\pi}\frac{g_m R_L}{C_T R_F}\frac{R_C}{R_E} = \frac{1}{2\pi}\frac{q}{kT}\frac{I_1(T) R_L(T)}{C_T R_F(T)}\frac{R_C(T)}{R_E(T)} \qquad (2)$$

where R_L is the load resistance of the first gain stage, R_C the collector resistance of the 2nd gain stage and R_E its emitter resistance. By taking the derivative of f_{3dB} with respect to T, one can determine the needed temperature coefficient of the current $I_1(T)$ such that f_{3dB} is independent of temperature at a given temperature T_0. Doing this, it turns out that the bandwidth over a large temperature is only weakly dependent upon temperature.

Simulation results

By zeroing the derivative of f_{3dB} with respect to temperature at T=50°C, it turns out that a bias current $I_1(T)$ with a negative temperature coefficient of -1.16 µA/°C minimizes the overall variation of f_{3dB} with temperature. Indeed, as shown on Fig. 3, this current gives a bandwidth of 187 MHz (this large bandwidth is needed to ensure a minimum bandwidth of 100 MHz in the worst case process corner) with a variation less than 8 MHz

over a temperature range of 180°C. Unfortunately, it turns out that this temperature coefficient is difficult to realize over different process corners. On a test chip, a temperature coefficient of -427 nA/°C was used, resulting in an acceptable variation of 25 MHz over a temperature range of 180°C. Also shown is the resulting bandwidth in case that a bias current is used that is constant with temperature, and a bias current that exhibits a positive temperature coefficient (e.g. a classical PTAT (proportional to absolute temperature) current source). It is clear that using a negative temperature coefficient results in less bandwidth variation with temperature.

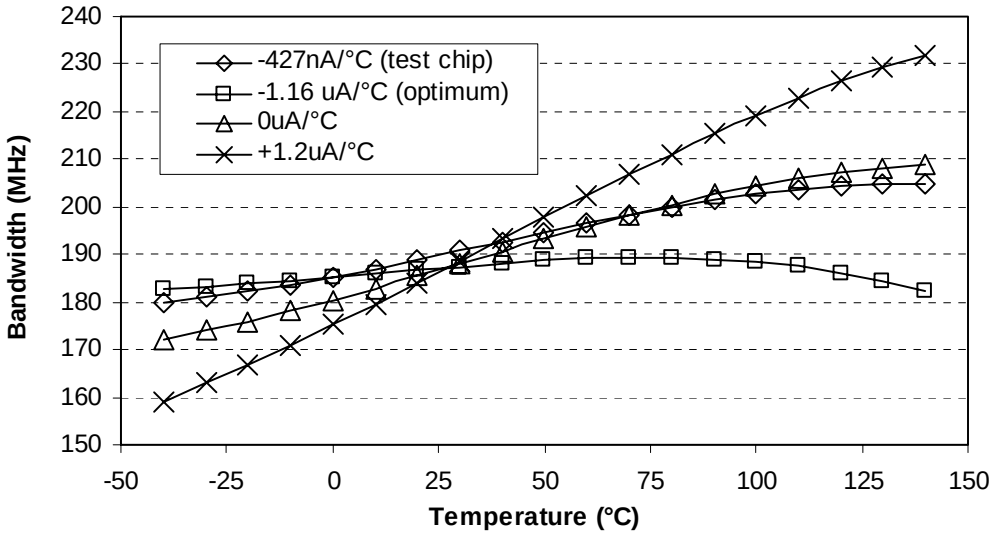

Figure 3 – Bandwidth as a function of temperature for different temperature coefficients.

Conclusion

Important considerations for the design of a highly sensitive optical Rx with integrated Si PD have been discussed. It is demonstrated how proper biasing of a TIA can reduce the variation of the bandwidth with temperature. This is important in order to maintain high sensitivity despite large temperature variations.

Acknowledgement

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References

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