

## Very high aspect ratio of photonic crystals holes in InP

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*We have used a three-level masking technique to achieve high aspect ratio photonic crystal holes in InP-based materials. The masking consists of a ZEP/Cr/SiO<sub>x</sub> stack where the ZEP layer is used to open the Cr which on its turn is a good mask for opening the 500nm thick SiO<sub>x</sub> layer. Subsequently InP is etched in an ICP process using Cl<sub>2</sub>:O<sub>2</sub> at a pressure of 1.4 mTorr. High aspect ratio could be achieved in holes ranging from 160 up to 330 nm in diameter with a maximum of 18 obtained with the narrowest holes having a diameter of 210 and 160 nm.*

### Introduction

Photonic crystals are extensively investigated for application in advanced photonic circuits. They offer better performance with reduced size. Low optical losses in planar 2D triangular lattice photonic crystals in InP can be achieved with deeply etched holes through an InP/InGaAsP/InP planar waveguide structure. The hole depth should be at least 1 μm below the Q-layer with smooth and vertical sidewalls [1-2]. Reducing the feature size influences directly the achieved etch depth: the smaller the hole, the shallower the depth. This phenomenon is known as RIE-lag [3].

Very good results of deeply etched photonic crystal holes in InP have been produced by Cl<sub>2</sub>-based chemically assisted ion beam etching [4-5]. CAIBE also suffers from lag effect for diameters well below 1 μm [6]. Good results of deep photonic crystal holes have also been accomplished by high plasma density RIE using ECR [7] and ICP [8]. Adding N<sub>2</sub> or O<sub>2</sub> to Cl<sub>2</sub> for sidewall passivation has been successful for the fabrication of deeply etched hole-type photonic crystals in the InP-based material system [9-12]. A limiting factor for achieving aspect ratios much higher than 10 is the mask erosion, for instance in [9-11] 400 nm of SiN<sub>x</sub> was used as a masking layer which allowed for an etching time of 1 minute. In the present paper we have investigated the use of a three-level masking technique to increase the mask thickness and using the same process as described in [10-11] we succeeded to extend the etching time to 2 minutes. This has resulted in a major improvement of aspect ratio of narrow holes in bare InP substrates up to 18. Furthermore as infiltration of PhC holes can be very interesting for tuning PhC bandgap [13] we have tested the infiltration of the obtained high aspect ratio holes.

### Experimental Results

All experiments were carried out on n-InP bare samples. The 3-level masking [13] consists of a 500 nm SiO<sub>x</sub> layer on which 50 nm of Cr is e-beam evaporated. The triangular photonic crystal holes patterning is performed by electron-beam lithography in a RAITH-150 system at 30 keV using 320 nm of the positive e-beam resist ZEP520A. Four different fields were patterned presenting lattice constants of 540, 460, 340 and 260 nm respectively while the air filling factor was maintained constant at 30%. A dose sweep was used to determine the optimal dose for each lattice constant.

After developing the PhC patterns the Cr is first opened in a  $\text{Cl}_2\text{-O}_2$  ICP plasma for 1 minute followed by a  $\text{CHF}_3$ -RIE process to open the thick  $\text{SiO}_x$  mask. We have intentionally over-etched the  $\text{SiO}_x$  to ensure a complete opening of the oxide layer in the smallest holes albeit the  $\text{SiO}_x$  layer in the largest holes may get an undercut profile that induce an extra roughness in the topmost of the holes. Ideally the oxide etching time should be optimised separately for every hole size.

Prior to the ICP etching of the deep holes in InP the residual ZEP, if any, and Cr were removed in an  $\text{O}_2$ -plasma to avoid micro-masking due to Cr sputtering. The etching process parameters are:  $\text{Cl}_2\text{:O}_2$  (14:2sccm), 1.4mTorr,  $200^\circ\text{C}$ , 1000W ICP, 160W RF power. The etching was carried out in a load-locked plasmalab 100 from Oxford Plasma Technology. The InP sample (few  $\text{mm}^2$ ) was glued onto a Si-carrier wafer by means of a heat sink paste. The use of He-backside cooling ensures a well defined sample temperature as compared to the electrode temperature.

The first tests show clearly that the  $\text{SiO}_x$  layer withstands better the ICP process than the  $\text{SiN}_x$  and that the etching time with 500 nm of  $\text{SiO}_x$  can be extended to 2 minutes.

Figure 1 shows PhC holes with a lattice constant of 340 nm ( $\varnothing$  200nm) etched for 1min and 30sec.

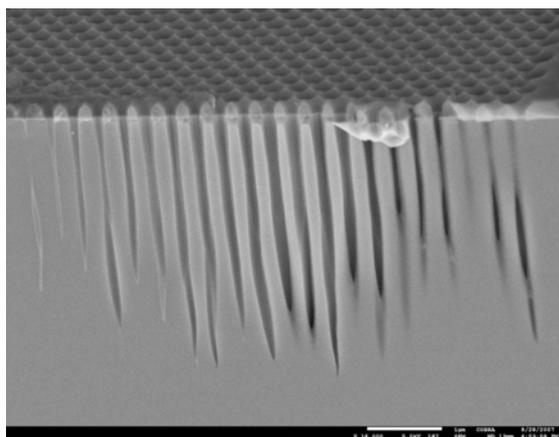


Figure 1- Etched field with 340-nm lattice constant and  $30\mu\text{C}/\text{cm}^2$  dose.

In the following experiments we have started the ICP process at an RF power of 100W and once the plasma was stabilized the RF power was increased to 160 W. This was done to avoid a possible ion scattering at the plasma ignition that may result in some under-etching visible on top of the holes.

Figure 2 shows two SEM micrographs of a sample etched in total 2minutes. The micrograph on the left shows holes with 340nm lattice constant and a hole diameter of 190 nm. The etch depth of a reasonably assimilated cylinder was estimated to be about  $3.40\ \mu\text{m}$  which results in an aspect ration of 18. The micrograph on the right shows the holes of the smallest lattice constant used i.e. 260 nm (hole diameter 160nm) with an estimated etch depth of  $2.90\ \mu\text{m}$  resulting in a surprising aspect ratio of 18.2.

To be noticed that the etched depth measured for holes with design diameters of 280, 210 and 160 nm were  $4.15$ ,  $3.40$  and  $2.90\ \mu\text{m}$  respectively. This result follows the well-known RIE lag rule; however the corresponding aspect ratios are 15, 17.9 and 18.2 respectively showing systematically higher aspect ratios with the two smallest lattice constants, i.e. 340 and 260 nm. This phenomenon is possibly related to the longer etching of the  $\text{SiO}_x$  masking layer that turns to be more beneficial for the fields with the smallest lattice constant.

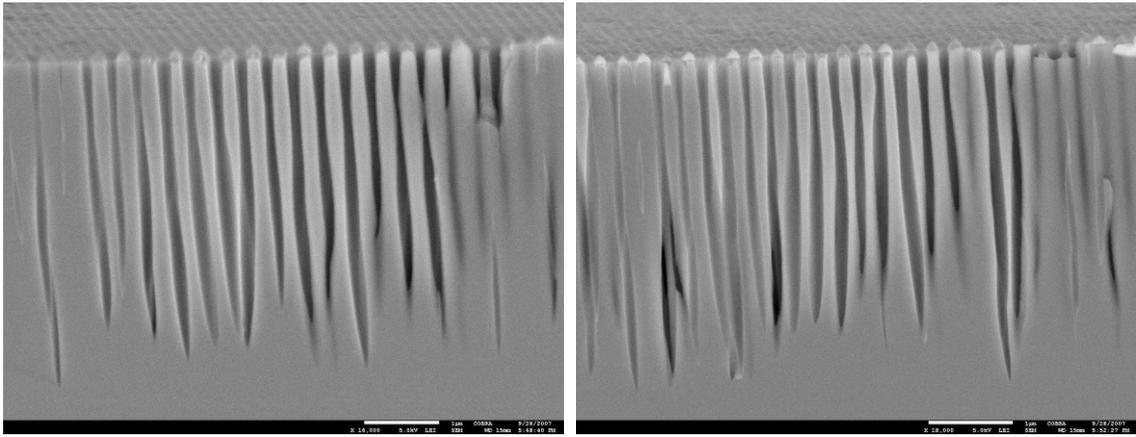


Figure 2- Holes of 190nm diameter at  $0.33\mu\text{C}/\text{cm}^2$  dose (left) and 160nm diameter at  $0.36\mu\text{C}/\text{cm}^2$  dose (right) resulting both in aspect ratios around 18.

An infiltration test with BCB was carried out to check its feasibility. The used sample was etched the same way as the sample shown in figure 2. After the ICP etch the remaining  $\text{SiO}_x$  masking layer was removed in a 10%HF solution. Subsequently a BCB layer (3022-46) was spun at 1500 rpm during 30sec and baked 2-minutes at  $120^\circ\text{C}$ . Figure 3 shows a cleaved plane of the 460 nm lattice holes demonstrating a good infiltration of BCB into the bottom of the holes.

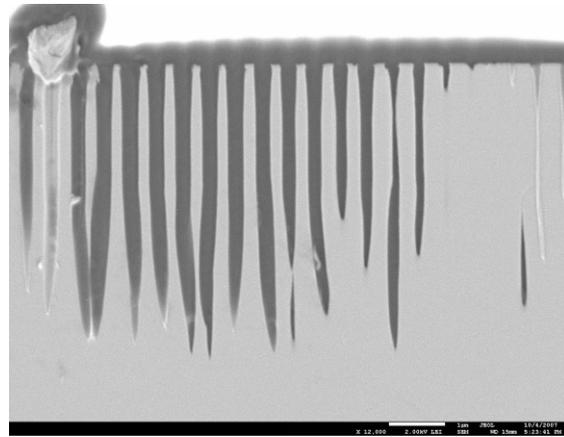


Figure 3- Infiltrated PhC holes of 280nm diameter with BCB.

## Conclusions

We have demonstrated a 3-level masking technique to manufacture photonic crystals holes in InP using a  $\text{Cl}_2\text{-O}_2$  ICP process. This technique appears beneficial to achieve very high aspect ratios ( $>18$ ), particularly in narrow holes with diameters of 210 and 160 nm. Furthermore, we demonstrated the possibility of infiltrating the deep holes with BCB which is very promising for tuning the PhC bandgap.

## Acknowledgements

This work is supported by the NRC-Photonics grant of the Dutch NWO. Peter Kaspar would like to thank ePIXnet for supporting his stay at the TU/e.

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