Low-cost packaging concepts for integrated nano-photonics

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Coupling an optical chip to its surroundings is very hard compared to an electrical chip. This complexity is mainly caused by alignment and accuracy challenges and is driving the cost price up to levels at which the commercial benefits of optical chips are no longer obvious, despite their many great technological advantages. Up to 80% of an optical system's cost price consists of packaging, in which the coupling of chip to fiber is done on chip level instead of per wafer. We investigate reducing these packaging costs to make optical chips commercially more attractive.

Introduction

Photonic Integrated Circuits (PICs) enable the realization of small-size optical circuits, using mature fabrication technologies well-known from the electronics industry. In particular in the last few years, foundry services have become available for the three main material systems: III-V semiconductors, Silicon-On-Insulator (SOI) and for dielectric systems such as Triplex^{TM}. The existence of these foundry services is a key enabler to reach low-cost, high-volume manufacturing according to standardized design rules. However, the optical interface of the PIC to the outside world is still cumbersome. It is essential to solve this. Compare the situation to electronics: who wants an electronic chip without bond pads?

Optical interface

Most applications in photonics require an optical interface. This holds in particular for telecom applications, but also for sensors. One of the key benefits of all-optical sensors, other than the small size and high sensitivity, is that they enable remote sensing without the need to worry about electrical interference. For example in Magnetic Resonance Imaging systems, or in the neighborhood of electric generators or internal combustion engines, all-optical sensors are a huge advantage.
If sources and detectors can be integrated with the optical circuit, no optical interface may be needed at all. This is possible in III-V based PICs, or by processing small III-V islands on a Si-wafer [1]. The main cost driver in this case is yield, which tends to decrease for each additional active device on the chip. The costs of bare III-V chip are often exaggerated. Referring again to electronics: applications which require high power and high speed are generally implemented in GaAs or InP, even in common consumer products such as mobile phones.

Scope

We believe that fiber-chip coupling is a must-have, even for most applications in III-Vs. For the next decade, the main applications of PICs will be in relatively low-cost, small-scale integration devices, which can be manufactured in high volumes. Large scale

integration is unlikely to become commercially attractive until optical functionality has become digital, so that the system performance is not limited by accumulated noise, crosstalk, jitter and back reflections. High volumes imply that packaging costs must be as low as possible, say less than EUR 10,-. Our vision is that SOI is the most promising platform for quick time-to-market for high-volume photonics, because of the relatively low costs per chip, and because of the matureness and scalability of its CMOS-compatible fabrication technology. For low-cost packaging of SOI PICs, we identify two main strategies: butt-coupling and the use of Vertical Grating Couplers (VGCs). Below we elaborate on their drawbacks and benefits.

Butt-joint coupling

Spot Size Converters

The mode in a waveguide is usually much smaller than the mode in a standard 9 um diameter single mode fiber. To improve the match, the waveguide mode can be expanded by means of a Spot Size Converter (SSC). This brings two benefits: first, the coupling loss is reduced, and second, the alignment tolerance is relaxed. Many reports on SSCs have been published, using vertical etches, shadow masks, inverted tapers, polymer or amorphous silicon over cladding etc, however, a commercially attractive solution is not yet available to our knowledge. We are investigating a number of SSC concepts for SOI ourselves, taking into account an outlook for high-volume manufacturing. Our concepts provide roughly 20% efficiency for coupling to a cleaved fiber, which we consider rather low, and may be published elsewhere in a later stage.

High-end

Butt-coupling for high-end applications usually involves a single lensed fiber (or a fiber with a GRIN lens) per chip facet. PICs that need two optical connections usually have these at two opposite facets. Often, the chip contains some form of SSC as well to have a good match to the still rather large spot in the lens focus. Coupling loss can be as low as 1 dB for perfect alignment, increasing to 3 dB for 2 um misalignment [2]. To achieve the sub-micron alignment that is needed for high-end lensed fiber assemblies, the actual chip performance is monitored during the alignment process (active alignment). The main cost drivers for this approach are the complex micro-mechanics in the package, the labor-intensive alignment procedure, and the cost of the fibers (few tens of Euros even in large quantities).

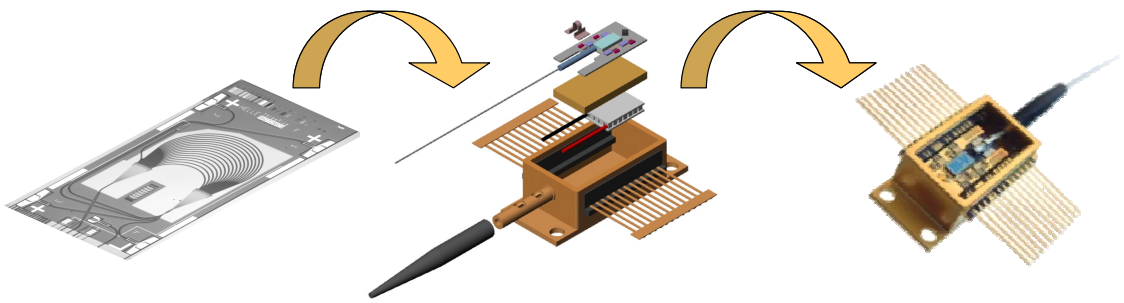

Figure 1: high-end butterfly package with lensed fiber butt-coupled to an InP chip,

Low-end

A simpler approach involves the use of as-cleaved fibers. This is only feasible with a large mode size waveguide structure or a proper SSC, or if the power budget is very comfortable. Due to the large mode size of the fiber, the alignment tolerance is relaxed. It also enables the use of fiber arrays, usually in wet-chemically etched Silicon V-grooves. Note that for a fiber in a V-groove that is not actively aligned, the excentricity of the fiber core (1 um typically) is a first hit to the assembly performance.

For V-groove based assemblies, it would seem beneficial to put the V-groove on the chip that also contains the optical circuit: alignment is done by litho, and only few components are needed. That has some drawbacks, however. First, fixing the fiber requires some length, typically in the mm-range. That is a lot of expensive chip real estate to sacrifice. Second, V-groove definition is a rather macro-scale process, which is difficult to combine in terms of processing with the nm-sized features, in particular the deep wet etch. Third, connecting the fiber does not involve alignment other than in the direction of the fiber. In case of trouble, there is no knob to turn to improve things.

The use of as-cleaved fibers is attractive for cost reasons, but other than the poor coupling efficiency we need to worry about reflections. As-cleaved fibers have a reflection coefficient of 4%, and should be connected to a chip that has its waveguides perpendicular to the facet. In many cases, reflections will have to be suppressed, and coating of the chip and/or fiber is needed, again increasing costs. Alternatively, angled-facet fibers can be applied to angled facet chips, however, this makes the solution more expensive.

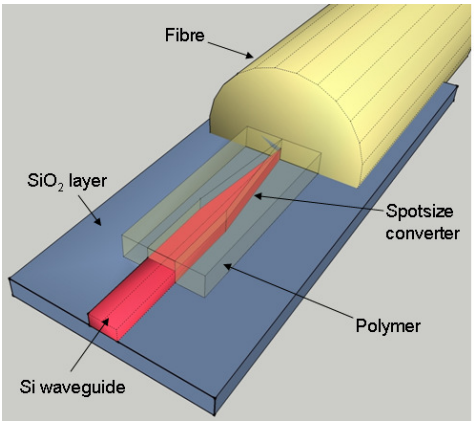

Figure 2: artist impression of a Spot Size Converter having an inversely tapered Si waveguides with a polymer over cladding.

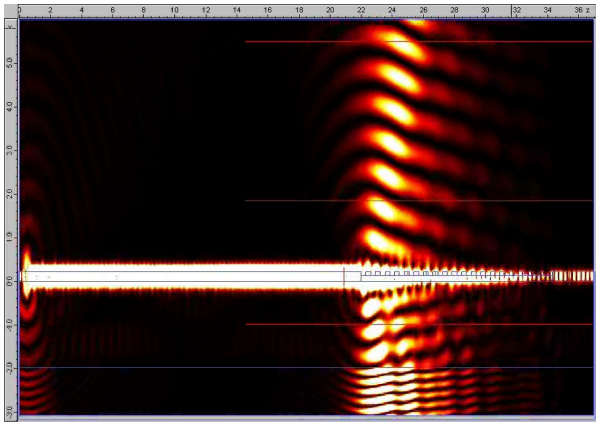

Figure 3: simulation of a Vertical Grating Coupler: light input from the left is directed upwards and downwards

Vertical Grating Couplers

Vertical Grating Couplers (VGCs) consist of a grating structure for which constructive interference is in a near-vertical direction. An excellent overview can be found in [3]. The coupling loss of a standard VGC to a cleaved fiber is in the order of 5 dB, or 30%, that is, under two conditions:

1. The polarization in the fiber is such that it perfectly matches the TE polarization in the waveguide. For coupling unpolarized light to a standard VGC, add 3 dB coupling loss. Advanced VGC configurations have been presented in [3] that

also couple the orthogonal polarization to the TE mode in a second waveguide, enabling implementation of polarization diversity, i.e. each polarization has its own optical circuit. This avoids the 3 dB penalty. Note that a typical SOI waveguide structure has such huge polarization dependence that splitting TE and TM is a wise thing to do anyway.

2. The fiber is very close to the chip. In practice, the light direction is 8-10 degrees off the normal direction, so in order to have the fiber core close to the VGC the fiber must have an angled facet. Even so, for as-cleaved fibers the loss does not increase much. The VGC can be equipped with a focusing feature to achieve better coupling to distant fibers.

The coupling loss can be improved substantially by introducing reflective boundaries that direct the downward propagating light upward, or by using a silicon overlay. The overlay is offered in the process library of Epixfab [4]. A further advantage of VGCs is that is allows on-wafer testing. A disadvantage is its limited bandwidth of typically 40 nm, however, this is sufficient for most applications. The off-normal direction of the input and output light is a difficulty in terms of package mechanics. Perpendicular coupling has been reported [5][6], however, fabrication tolerances are tight, and process deviations will not only affect the coupling efficiency but also affect back reflections, likely detoriating the chip performance.

Conclusion

It is essential to reduce the cost of fiber-chip coupling to enable commercial application of photonics. We study the feasibility of butt-joint coupling, and identify the absence of an easy-to-manufacture well-performing Spot Size Converter as a potential show stopper. The alternative coupling scheme based on Vertical Grating Couplers seems more attractive to us. In most cases, the limited bandwidth and polarization dependence are acceptable. The key is mainly to design a low-cost mechanical solution that is manufacturable in large quantities, and to develop the manufacturing tools for this, which is a subject we are currently looking into.

References

[1] Joris Van Campenhout, Liu Liu, Pedro Rojo Romeo, Dries Van Thourhout, Christian Seassal, Philippe Regreny, Lea Di Cioccio, Jean-Marc Fedeli, Roel Baets, 'A Compact SOI-Integrated Multiwavelength Laser Source Based on Cascaded InP Microdisks', Photonics Technology Letters, Vo.20,No 16,1345 - 1347, 2008.

[2] W.Hunziker, 'Ways to cost effective packaging: waveguide tapers and passive self-alignment', IEEE LEOS 98 Orlando,Vol.1, 36-37,1998.

[3] G. Roelkens□, D. Vermeulen, F. Van Laere, S. Selvaraja, S. Scheerlinck, D. Taillaert, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, 'Bridging the Gap Between Nanophotonic Waveguide Circuits and Single Mode Optical Fibers Using Diffractive Grating Structures', Journal of Nanoscience and Nanotechnology, Vol. 10, 1551–1562, 2010

[4] http://www.epixnet.org/

[5] Günther Roelkens, Dries Van Thourhout, Roel Baets, 'High efficiency grating coupler between silicon-on-insulator waveguides and perfectly vertical optical fibers', OPTICS LETTERS, Vol. 32, No. 11, 1495-1497, 2007.

[6] Xia Chen, Chao Li, Hon Ki Tsang, 'Two dimensional silicon waveguide chirped grating couplers for vertical optical fibers', Optics Communications 283 (2010) 2146–2149.