Towards a fibre to waveguide coupling scheme

J.H. van de Berg, R.A. Nieuwland, P. Bodis, P.J. Harmsma, K. Agovic and M. Yousefi

TNO Science and Industry, P.O. Box 155, 2600 AD Delft, the Netherlands

Silicon based SOI PICs are finding new applications in the field of sensing. Since Silicon does not produce light, to deploy these sensors in real-world applications a fiber-chip connection is required. In this work we detail the fabrication of V-grooves for fiber attachment to the chip, including the design, (hard) masking and the etching process. Our results show that V-groove attached fibre is an optimized solution for SOI based sensor PICs.

Introduction

Moving into the optical age of silicon [1] the need for cost effective connections into and from the Photonic Integrated Circuit (PIC) is becoming more stringent. The advantage of CMOS compatible production technology for PICs draws attention from manufacturers of various kinds of sensor technologies. The benefits of both a small sized sensor and most importantly the low-cost mass produceability of the PICs are of considerable interest. The approach however, differs from the current standards. PIC based sensors are envisioned a consumable or disposable product which is ultimately accessible to everyone. Such an approach requires a connection to the outside world which is both accurate and cost effective. This paper deals with the fabrication of v-grooves for fibre attachment to the chip. In addition, a quantitative comparison of the v-groove fabrication tolerances versus the horizontal and vertical misalignment penalty for a laterally tapered spot size converter is given.

Fibre to SOI waveguide coupling tolerances

The fibre to chip coupling from and to a Silicon on Insulator (SOI) based PIC is based on a laterally tapered design as given in [2] and an artist impression is given in Figure 1

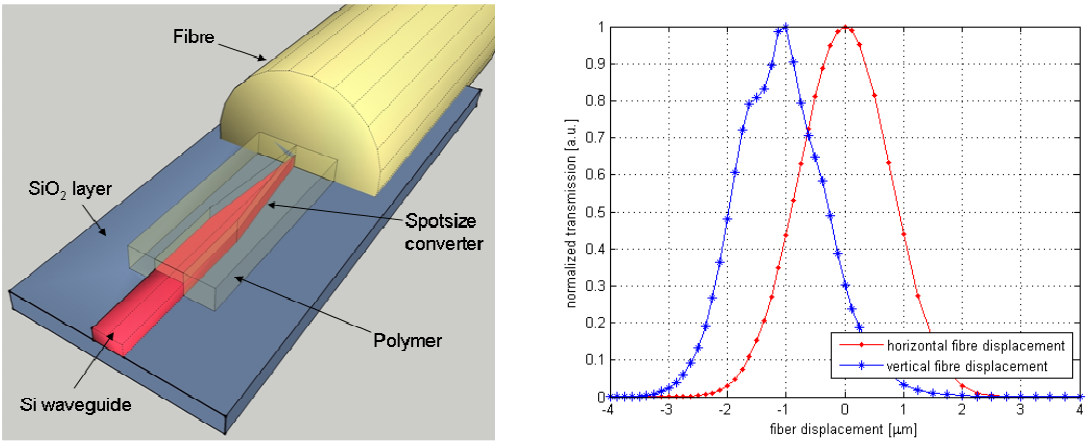

Figure 1: artist impression of laterally tapered spot size converter design (left) and FTDT simulations of fiber displacement with respect to the spot size converter (right)

(left). FTDT simulations indicate horizontal and vertical offset tolerances of ±1 μm to obtain <3 dB coupling efficiency, see Figure 1 (right).
Alignment of the fibre with respect to the spotsize converter in horizontal and vertical position is possible using v-grooves which restrict the fibre position. The v-groove location accuracy with respect to the spot size converter is dominated by the accuracy of the mask aligner and estimated to be in the order of 0.2 μm. The vertical accuracy of the fibre with respect to the spot size converter is governed by the v-groove depth which in turn is restricted by the fabrication process tolerances.

V-groove technology for fibre attachment to PIC

Planar SOI PIC consists of a Silicon wafer which is topped by a 1 to 2 μm layer of silicon oxide and finally capped by a thin (200 to 300 nm) layer of Silicon. This last layer is the device layer and contains the PIC. The dimension of a typical single mode Silicon waveguide is around 450×220 nm. Integration of active components like lasers and/or detectors using Silicon is not straightforward, therefore light is led from and to the SOI PIC using optical fibre. The optical fibre is usually 125 μm thick with a core of 9 μm at the centre of the fibre. The purpose of the V-groove is to align the fibre on the PIC, such that the field overlap between the fibre mode and spotsize converter is maximized.
In the TNO fibre-waveguide connection scheme the Silicon waveguide is tapered laterally towards a point which will push the field outwards to a polymer buffer layer.
Using a spot size converter instead of simply direct butt coupling of the Silicon waveguide to the fibre has two more advantages. Firstly the spot size converter dimensions are a closer match to the fiber core dimensions compared to the small Silicon waveguide. This in turn, relaxes the alignment tolerances of the fibre with respect to the spot size converter. In addition, the modal field conversion by tapering down the silicon waveguide results in a reduction of the coupling losses.

According to [3] the size, angle and depth of the V-groove can be estimated in a straight forward manner. Figure 2 shows a sketch of the setup. The dimensions needed to calculate the height, *h*, of a fibre core above the silicon substrate as a function of the width, *W*, of a v-groove etch mask opening is shown in Figure 2. Additionally, *d* is the depth of the v-groove that is etched in the silicon substrate, *r* is the fiber radius and 2θ is the v-groove angle defined by the crystallographic planes of the Silicon substrate in the 111) direction, the faces of which act as an etch stop in the wet etch process.

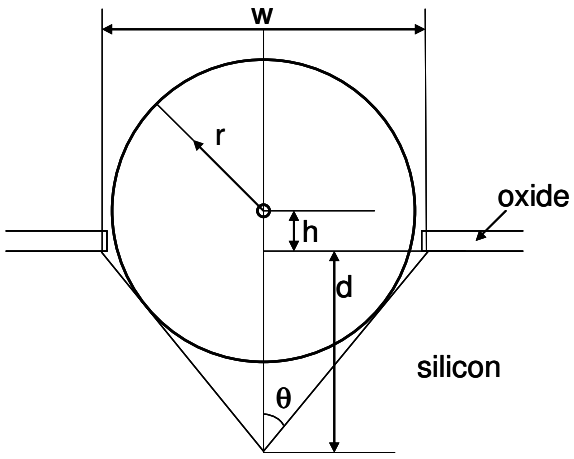

Figure 2: Schematic representation of the v-groove with fibre.

For a given crystalline orientation, the v-groove angle will remain constant meaning that additional wet-etching will lead to a deeper and wider groove. Therefore, by regulating the etch mask width (W), the depth of the v-groove can be controlled so that the center of the fiber core is aligned to the waveguide of the planar PIC. Note that different crystalline directions, such as (100) or (110) will result in different angles.

More accurately, the depth d is given by

$$d = \frac{W}{2\tan(\theta)}, \tag{1}$$

and the relative displacement of the core with respect to the top of the silicon wafer is given by

$$h = \frac{r - d\sin(\theta)}{\sin(\theta)}. \tag{2}$$

In our case we will use the top oxide layer as the etch mask. Thus, given a certain width of the mask opening in the silicon oxide layer, we can calculate the location of the center of the fiber core ($h + d$) with respect to the bottom of the v-groove. Note further that d is a function of the etch time thus leaving us with the only free parameter h.
The fabrication accuracy of the v-groove depth is determined by the width of the mask, W and is related to the depth by Equation (1). The accuracy of the width, W is defined by the optical lithography step in the fabrication process and determined using SEM images to be around 1 μm. Using Equation (1) and assuming a 45° v-groove angle results in a fibre core location variation of 0.5 μm.

Wet chemical etching of Silicon

Strong alkaline substances (pH > 12) such as aqueous KOH-solutions (potassium hydroxide dissolved in water) etch Si via:

$$Si + 4\ OH^- \rightarrow Si(OH)4 + 4e^-.$$

Since the bonding energy of Si atoms is different for each crystal plane, and KOH etching is not diffusion- but etch rate limited, Si etching is highly anisotropic: While the (100)- and (110)-crystal planes are being etched, the stable (111) planes act as an etch stop.
The degree of anisotropy (etch rate selectivity between different crystal planes), the etch rates, and the etching homogeneity depends on the temperature of the reaction, atomic defects in the silicon crystal, intrinsic impurities of the Si crystal, impurities (metal ions) in the etchant, and the concentration of Si-atoms already etched. The doping concentration of the Si also strongly impacts on the etching.
KOH solution can etch the (100) plane 400 times faster then the (111) plane, depending on the exact temperature and concentration of the solution. One of the drawbacks of this chemistry is its incompatibility with CMOS processing, due to the presence of K+ ions after the etch. Care must therefore be taken to establish a processing scheme in such a way that the KOH etch is one of the last processing steps and does not cause contamination of the CMOS line.
By appropriate orientation of the etch window in the hard mask with respect to the (111) plane, slots can be etched into a (100) Silicon wafer that are triangular in cross section, with the sides determined by the (111) planes and that meet the (100) plane at an angle

of 54.7°. In order to obtain a 45° angle the (110) planes can be utilized as the etch-stop planes rather than (111) planes.

Results

Given the above stated recipe, V-grooves with the sides determined by the (111) plane are etched into SOI wafers. V-grooves at an angle of 54.7° are produced and a standard single mode fibre is glued into the groove, see Figure 3. Using the larger angle increases the manufacturing accuracy of the v-groove depth to ~0.35 μm. Combined with the V-groove location (with respect to the SOI waveguide or spot size converter) an error of 0.2 μm is accurate enough to allow <3dB fiber to chip coupling losses.

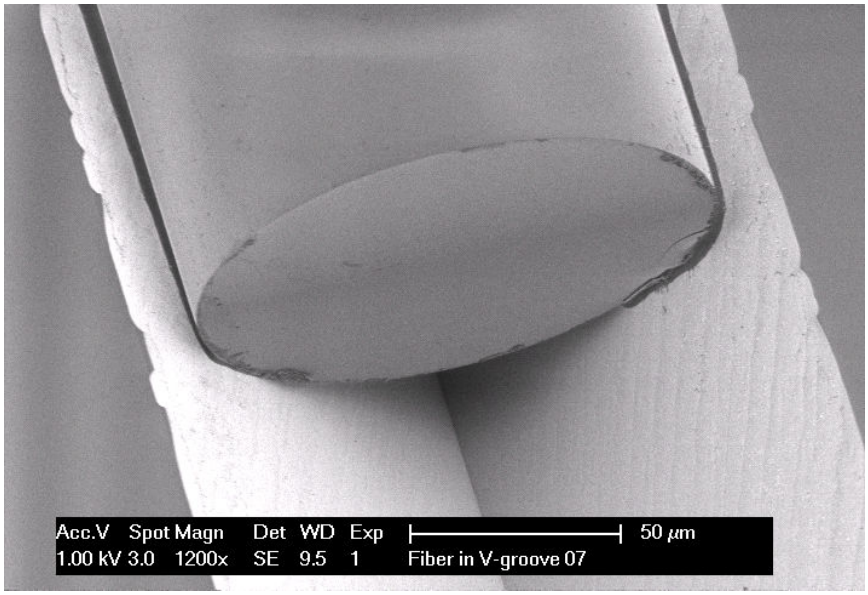

Figure 3: SEM image of fabricated v-groove with glued fibre

References

[1] G. T. Reed, "The optical age of silicon," in Nature 427, 615–618, 2004.

[2] G. Roelkens, P. Dumon, W. Bogaerts, D. van Thourhout and R. Baets, “Efficient Siliocn-on-Insulator Fiber Coupler Fabricated Using 248-nm-Deep UV Lithography,” in IEEE Photonics Technology Letters, vol. 17, 2613-2615, 2005.

[3] C. Raum, D. Duguay, C. Elliott and R. Gama “Process Characterization of (110) Aligned Silicon for V-groove Formation”, Zenastra Photonics Inc.