Integrated Optical Switch Circuit Operating under FPGA Control

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Integrated photonic circuits are enabling an abrupt step change in networking systems providing massive bandwidth and record transmission. The increasing complexity of high connectivity photonic integrated switches requires sophisticated control planes and more intimate high speed electronics. Here the first demonstration of a fabricated twenty-electrode broadcast-and-select photonic integrated switch controlled by a field programmable gate array (FPGA) is presented. Multipath 10 Gb/s data routing with rotating and pseudorandom priority path arbitration is assessed. Dynamic routing for $2.4x10^6$ packets per second through all the working paths of the photonic integrated switch is shown using only a single external clock signal input.

Introduction

Massive bandwidth data links and fast reconfigurable optical interconnects requirements have encouraged a considerable integration of photonic circuits to minimise losses, delays, size and energy consumption. State-of-the-art photonic integrated switches are being designed, fabricated and demonstrated for future ultrahigh-bandwidth low-latency computer interconnects [1]. Record routing of 320 Gb/s data rate in multistage integrated circuits [2] and increasingly high connectivity integrated switched networks [3-4] have been accomplished. However evaluation of photonic integrated circuits (PICs) has so far been predominantly limited to device level characterization [3-5]. The first example of a dedicated scheduler for full routing control for a twenty-electrode photonic chip and complex electronic plane has been recently demonstrated [6]. However automated full routing control of photonic integrated switches still represents a challenge, due to the required high-speed and simultaneous control of input and output data. In this work, the first reconfigurable routing control protocol of a twenty-electrodes photonic integrated switch is presented. The photonic complexity is abstracted by a field programmable gate array in the control plane which requires only one single time-slot clock signal input and allows for both rotating and pseudo-random path selection. The desired scheduling protocol is implemented for the first demonstration of multipath routing on a PIC, with an important system-level simplification for photonic circuit performance, and considerable hardware reduction.

Switch Fabric

The experimental control plane to demonstrate automated multipath data routing is schematically shown in Fig. 1. A field programmable gate array (FPGA) logic, Virtex 5, is employed as a scheduler to enable the desired path arbitration. The FPGA can be programmed to perform different protocols and control algorithms. The very-high-speed integrated circuits hardware description language (VHDL) is used to describe the digital

system. After the synthesis and simulation of the code, the design is placed and routed to fit into the target FPGA. A second simulation is performed to help establishing how well the design has been placed and routed. Finally, the generated design is loaded onto the FPGA. An internal buffer composed of sixteen latches synchronizes and conditions the signals which are then sent to the nanosecond speed current drivers. For convenience, the clock signal at the input of the scheduler is derived from the same pulse pattern generator, which is used for data generation. A level control block, shown at the top right of Fig.1, defines the current signals to each of the twenty electrodes.

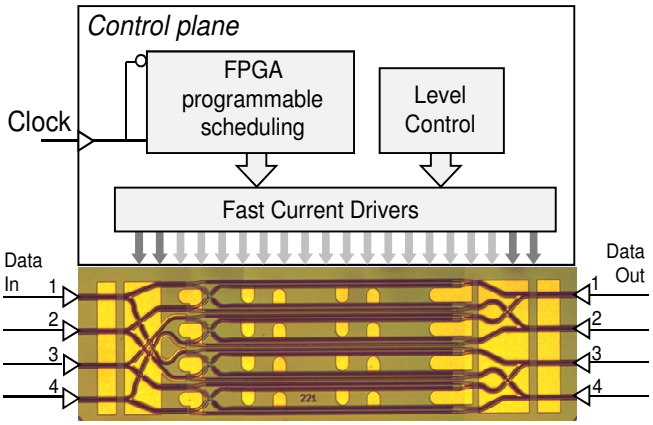

Fig. 1 – Sophisticated switch fabric highlighting the photonic integrated circuit and its control plane.

The controlled photonic integrated switch is shown at the bottom of Fig.1. This is a twenty-electrode, four-input, four-output, broadcast-and-select, semiconductor-optical-amplifier (SOA) based switch fabricated from quantum well active epitaxy. The total area of the integrated circuit is only 4×1 mm^2, providing sixteen paths addressable by biasing the appropriate gate SOAs. Required operating currents are in the range from 120 to 150 mA. There is spectral evidence of waveguide damage for six paths which are lossy and unused in this work. Physical layer assessment reported in [6] shows that fibre-to-fibre gain is limited by facet reflections and the on-chip gain therefore compensates the losses due to the splitters and combiners. Antireflective coatings will allow significantly higher gain. The path crosstalk values for this circuit are measured to be within the range from -29.1 to -42.5 dBm and a power penalty of 2.6 dB is measured for data routed over a typical path of average length [6].

Multipath Routing Set-up

Automated scheduling is implemented to show multipath routing assessment for the PIC. The experimental arrangement is depicted in Fig. 2. The dynamic routing of the ten viable paths allows the full verification of all the input and output ports for the sub-system. A 10 Gb/s pseudo random bit sequence (PRBS) of 2^7-1 bits is used to modulate the optical signal at each input of the PIC. This optical signal is routed through biased optical paths. A 409.6 ns (2.44 MHz) time-slot synchronization signal is derived from the same pulse pattern generator which is used for data generation and is sent to a Stanford pulse generator to provide a well-defined external trigger signal. This module generates the required differential clock signal and a reset signal used to tune the guard band duration for time trace inspection. The FPGA outputs all the sixteen differential digital signals for the fast current driver circuits which control the SOA gates. The

FPGA is programmed to generate the trigger signal to an oscilloscope for time trace inspection also.

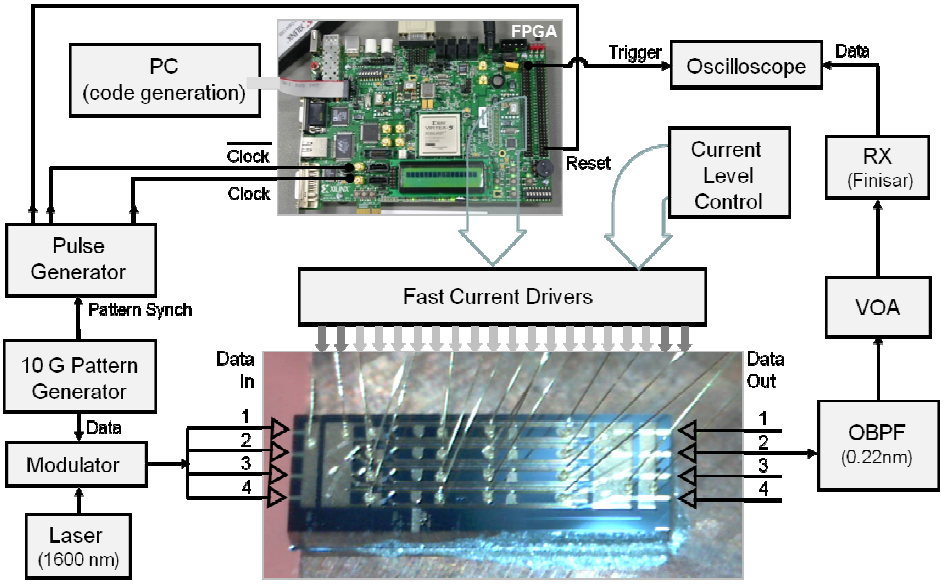

Fig. 2 – Schematic for multipath routing assessment set-up.

The control and test scheme for the photonic integrated switch is shown in Fig. 2. The input wavelength is set at the 1600 nm gain peak and modulated with 10 Gb/s PRBS data. The optical data signal is broadcast to all the switch inputs with a fibre splitter network and a fibre lens array with 250 μm pitch and is then coupled out through an individually manipulated single lensed fibre. Paths are selected in time through synchronized electronic control of the SOA gates. Each output port is assessed by scanning the output fibre lens. The output optical signal is then filtered with a 0.22 nm bandwidth filter for broadband noise rejection and converted into an electrical signal through a Finisar. Time traces for routed data are displayed on the scope.

Simulated Control Signals and Actual Routed Data

Dynamic routing of data at a packet rate of 2.4 MHz is demonstrated through all the working paths of the photonic integrated switch. Two arbitration schemes are implemented: (a) rotating and (b) pseudo-random priority path arbitration. Fig. 3 shows the timing diagrams for the simulated outputs of both arbitration schemes (above) and the correspondent resultant time traces of the routed data (below). In both (a) and (b) cases, the signals present at the input of FPGA are the differential clock and the reset signal. For each time slot, a sixteen bit instruction over the output bus is generated by the FPGA. Every instruction consists of four bits equal to "1" out of sixteen, so that during every time slot inputs are connected to all the outputs without packet contention. The rotating scheduling is implemented in the FPGA by using Johnson decade counter logic blocks, while the pseudo-random path selection algorithm is based on left shift feedback registers, 16 bits length and polynomial feedback $x^{16}+x^{15}+x^{14}+x^{5}$. The bottom part of Fig. 3 shows the time traces of the routed data corresponding to rotating priority (a) and pseudo-random path selection (b) respectively. Considering output 2 under rotating priority scheduling, each packet is routed in order from input 2, 3, 4 and 1, and then back to input 2. The trigger signal period for the scope at the output of the FPGA is

one fourth the input clock signal. Considering output 4 under pseudo-random path selection, packets are pseudo-randomly routed from input 1, 2 and 3. The trigger signal period to the scope has a period of one sixteenth the input clock period. The optical signal, modulated with 10 Gb/s 2^7-1 long packets of approximately 400 ns duration time are interleaved with artificially long 30 ns guard band durations for improved packet visibility.

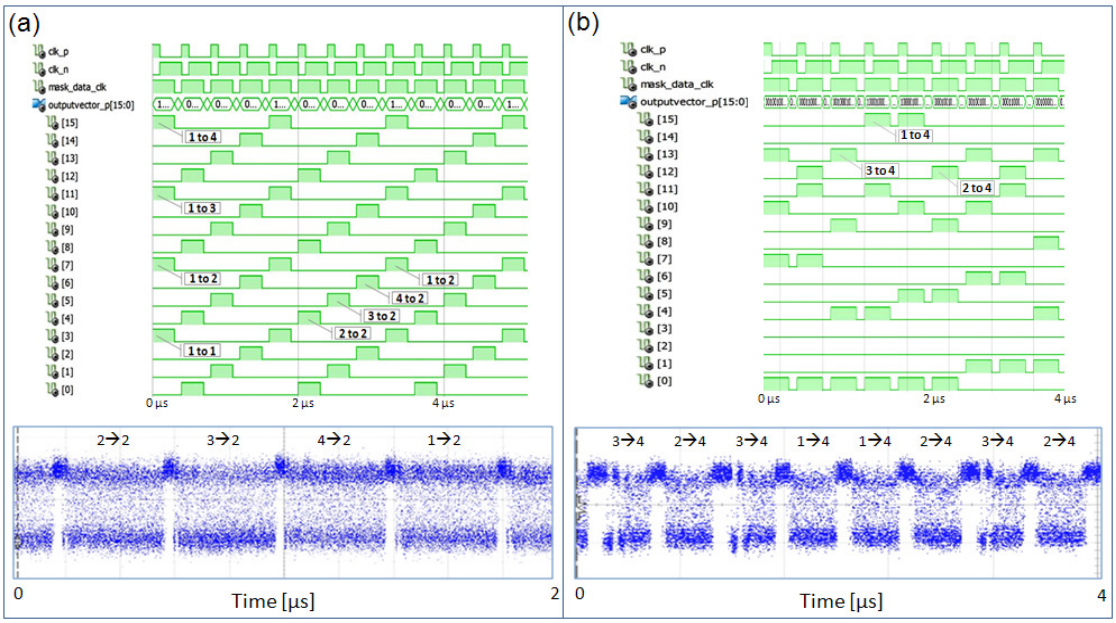

Fig. 3 – Top: simulated time traces from rotating (a) and pseudo-random (b) path selection. Bottom: time traces of the optical routed data in the case of a rotating (a) and a pseudo-random (b) path selection.

By investigating the switching transition, the guard band duration may be reduced to 10 ns without incurring visible errors in the sampled time traces. Good equalization of the output powers from the different paths is required to recover data at the receiver. The time traces shown at the bottom of Fig.3 show well resolved data packets.

Conclusions

Multipath routing using rotating priority and pseudo-random path selection protocols has been demonstrated for the first time for a twenty-electrode integrated switch. The control plane to dynamically route between four inputs and four outputs with 400 ns duration slot clock employs an FPGA. The total functionality of the chip has been demonstrated with only a single clock signal input.

Acknowledgements

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