Light Turning Mirrors in SiON Optical Waveguides for Hybrid Integration with CMOS Photo-detectors

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A new method is proposed for hybrid integration of SiON optical waveguides and standard CMOS photo-detectors based on anisotropic etching of 45° facets in a Si substrate. After removal of anisotropically etched Si structures in cladding SiO_2, the fabricated total-internal-reflection mirrors can direct the output of the waveguides to photo-detectors placed on top of the chip. The metal-free fabrication process, designed to create these mirrors, is convenient for batch production. Fourier optics based simulations predict that the reflection efficiency of the mirrors is 68.5 %. The far field pattern obtained from the fabricated device is similar to the simulated one.

1. Introduction

In recent years, waveguide (WG) based integrated optic devices have been used in many applications such as optical spectroscopy, biological sensing and medical imaging. Although all these WG based devices are very functional, they are not standalone useful. The optical data in the output WGs of these devices should be transmitted to optical detectors in order to get useful information. This transmission can be either done by using a bulky optical setup at the output of the optical chip or by making a hybrid connection between the optical chip and the electronic chip which contains monolithic photo-detectors (PDs). In order to realize small size and high functionality optoelectronic devices, hybrid integration option is very convenient. A number of techniques have been reported to provide such a connection. One of these uses a focusing grating coupler on top of a WG to focus the light onto the PD that is placed above the WG [1]. However, this device can only work for a limited wavelength range which is defined by the grating period. In addition, high volume production of this grating is not possible because no mask can be used to fabricate it, owing to its relatively small period. Another technique uses focused ion beam milling (FIB) for fabricating total internal reflection (TIR) mirrors at the end of silica WGs [2]. However, this technique is also not suitable for high volume production since only one mirror can be fabricated at a time by using FIB. The third technique is based on a metal mirror, at which the desired mirror angle is fabricated by using a superficial layer in the wet etching process of the buffer layer [3]. Although the efficiency of these mirrors is very high, the thermal budget of the fabrication process is low because the melting temperature of metal layer used in the mirror is relatively low.

In this paper, we propose a new method for the efficient integration of SiON optical WGs with CMOS based PDs, enabling 2D-arrangements of PDs. This method uses a TIR mirror for directing the output of the WG onto a PD. The fabrication process, which is designed to realize these mirrors, is convenient for batch production and it has a thermal budget of 900 °C. The mirror is considered to be formed at the interface between cladding oxide and air. The angle between surface normal of the mirrors and WGs is chosen to be 45°. This angle is sufficient to lead to TIR on the mentioned interface and it also provides perpendicular incidence onto the PDs.

The rest of this paper is organized as follows. First we will introduce the fabrication process steps designed for realizing the TIR mirror. Then, we will explain the simulations that are performed for estimating the mirror performance. After that we will show the device fabrication results. Finally, we will give a brief overview of the measurement results that are done on the fabricated devices.

2. Fabrication Process

The wafer cross-sections corresponding to different steps in the fabrication process flow is shown in figure 1-(a) through 1-(j). The fabrication process starts with 200 nm thermal oxide growth to be used as anisotropic Si etching mask. After that the oxide is patterned by using buffered HF (BHF) etching (1-a). This is followed by 5 µm anisotropic etching of Si (1-b). This depth is defined by considering the required thickness of the buffer layer. The thickness of the buffer layer should be 3.5 µm to prevent the substrate losses. The etch depth is 1.5 µm higher than the buffer layer thickness because it is necessary for proper overlap between the diverging WG output and the mirror surface. A TMAH and Triton mixture is used as an etchant to form the special walls that have an angle of 45° with the surface of the substrate [4]. The fabrication process is continued with removal of thermal oxide in BHF. Then, a 100-nm thick SiN layer is deposited (1-c) just before buffer layer in order to prevent the interaction between the buffer layer and the Si substrate. After that a thick Boron Phosphorous Doped Silica Glass (BPSG) film is grown to form the buffer layer (1-d). The BPSG is used in this step because it is possible to get rid of the voids in the as deposited layer by post- deposition annealing [5]. The thickness of the BPSG buffer layer should be at least 5 µm, which is equal to the etch depth defined in the anisotropic Si etching step, in order to be able to obtain a flat surface using CMP (chemical mechanical polishing) step. The BPSG layer is annealed just after deposition at 900 °C for 16 hours. The annealing step is followed by CMP step (1-e). Subsequently the BPSG is thinned in BHF solution such that a 3.5 µm thick buffer layer will remain between the guiding SiON layer and Si substrate (1-f). This is followed by the deposition and patterning of the core SiON layer, which has a refractive index of 1.585 (1-g). After that cladding BPSG layer is deposited, annealed and polished (using CMP) by using the same process conditions applied for the buffer BPSG (1-h). Then the isotropic Si etching holes are introduced on top of the elevated Si structures (1-i). Finally, the isotropic Si etching is done through these holes (1-j). In this step XeF_2 gas phase etching is used to selectively remove Si. By removing the elevated Si structures, 45° TIR mirrors are created.

The performance of the proposed TIR mirrors is estimated by using a Fourier optics based simulation. The mirror structure used in this simulation is simplified by ignoring the residual SiON layer on the 45° angled wall since the index contrast between BPSG and SiON is very low. Figure 2-(a) shows the cross-section of this structure. In this simulation the components calculated by Fourier decomposition of the WG mode are propagated through the TIR mirror and dielectric layer stack on the PD (PD). At the end, all of these propagated Fourier components are added to find the output intensity profile on the detector surface. Figure 2-(b) shows the intensity profile on the PD surface. As it can be seen from the figure, the intensity profile is not symmetric. This is because of the fact that symmetric Fourier components of the output beam makes different angles with the mirror and it results in different reflection coefficients. The

efficiency of the mirror is calculated to be 68.5 % since some of the Fourier components do not show TIR.

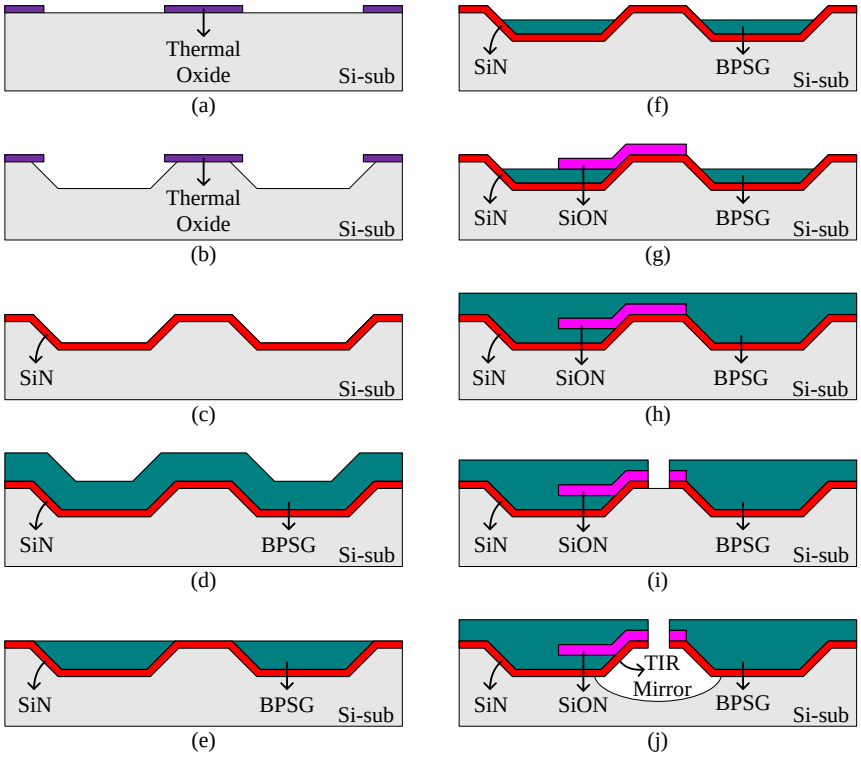


Figure 1: Wafer cross-sections corresponding to different steps in the fabrication process flow.

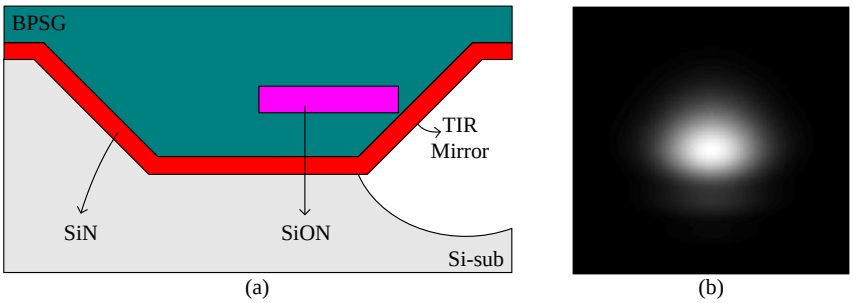
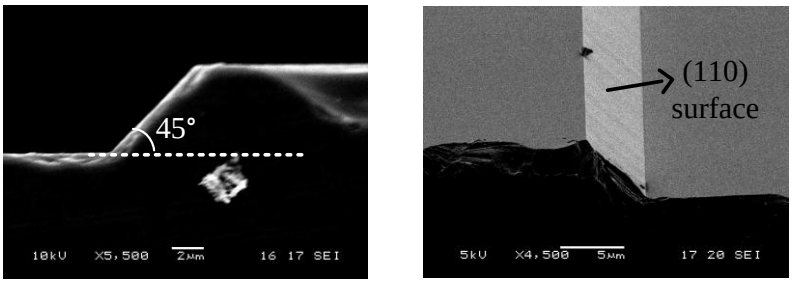


Figure 2: (a) cross-section of the simplified mirror structure used in the simulation and (b) calculated intensity profile on the PD by using this structure.

3. Optimization of the used Fabrication Process Steps

Anisotropic Si Etching: Triton x-100 added TMAH solution is used in this step. Concentration and temperature of this etchant are optimized in order to minimize the roughness on the etched (110) surfaces. Figure 3 shows the SEM pictures of Si structures that are made by using this optimized etching process. As can be seen from figure 3-(b) the etched (110) surfaces are not perfectly smooth. The effect of this roughness is investigated by doing an optical experiment. In this experiment a laser beam at 632 nm wavelength is focused on the etched Si surface and the reflected light from this surface is compared with the light reflected from the bare Si wafer surface. The measurement results show that the roughness degrades the reflection efficiency of the Si surface only 4 %.



(a) (b)

Figure 3: SEM Cross section (a) and top (b) view of Si structures etched in the optimized Si anisotropic etchant.

BPSG Deposition: The BPSG layers are grown by using PECVD method. Since as deposited BPSG layers grown by this method contain slits at the corners of pre-patterned layers (elevated Si structures in our case). Post deposition annealing is used to overcome this problem.

CMP of BPSG: The surface topology formed after anisotropic Si etching step maintains after the BPSG deposition. In order to remove elevated structures CMP is done after annealing the BPSG layer. Although the removal rate is higher in the non-annealed BPSG, we did the polishing after annealing because the non-annealed BPSG is attacked by the cleaning solution (RCA-2) used after the CMP process.

Isotropic Si Etching: Gas phase XeF_2 etching is used in this step. The selectivity of this etching step to annealed BPSG layer should be very high in order not to destruct the surface of the TIR mirrors. The experimental results show that the selectivity of XeF_2 etching to annealed BPSG is around 1500.

4. Conclusions

After optimizing all the steps of fabrication process, TIR based light turning mirrors for hybrid integration of SiON WGs and CMOS based photodiodes are successfully fabricated. Measurement results obtained from the fabricated device show that the efficiency of the mirrors are 47 % while the calculated efficiency is 68.5 %. The degradation is due to the problems in the fabrication process. These problems can be solved by changing the WG geometry.

5. References

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