Integrated optical serializer fabricated in a multi-project wafer run

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We present an integrated optical serializer designed and fabricated in a multi-project wafer run on indium-phosphide(InP)-based materials. The circuit is designed for a front-end unit in a data readout system. The InP-based technology platform enables monolithic integration of passive and active components. The serialization is provided by means of on-chip optical delay lines. The circuit makes use of electro-optic phase shifters to build amplitude modulators, multimode interference couplers for signal distribution, semiconductor optical amplifiers for signal loss compensation and on-chip reflectors. In this work we present the design and first experimental results of the fabricated device.

Introduction

We believe that photonic integrated circuits (PICs) will replace their bulk fiber optic or electrical equivalents in the coming years. The main advantages of PICs are their low power consumption, higher speed, compactness, better reliability and easier and cheaper maintenance. However, the major obstacle which has not been overcome so far is lack of a standard technology for PIC fabrication. Such a technology could enable a low-cost production of the photonic devices which could be applied in many fields such as tele- and datacommunications, medicine, sensing, metrology and others.
One of the potential solutions to make a breakthrough is a generic integration technology. The idea is to develop a set of basic building blocks (BBs) which are used in a design of a more complex PIC and could be fabricated in a single process. These blocks are, for example, a waveguide, a phase modulator, a semiconductor optical amplifier (SOA) and a polarization converter. A very important feature of this concept is that PICs designated for various fields of application may be designed and fabricated in the very same technology process. This will result in significant cost reduction for fabrication of photonic ICs.
The EU FP7 project EuroPIC aims to develop such a standard, generic technology for an indium-phosphide(InP)-based technology platform. The advantage of InP is that it enables monolithic integration of passive and active devices. Within the framework of EuroPIC, ten pilot application-specific photonic integrated circuits (ASPICs) are being designed and fabricated in multi-project wafer runs. The application areas of these ASPICs are telecommunications, medicine, sensing and data readout.
The concept of a multi-project wafer (MPW) run was developed for silicon microelectronics and it enables access to that technology also for small-scale projects. In such an MPW, the wafer space is shared between different users that each design their own cell. The same idea is now being applied in photonics. COBRA Research Institute already offers a small-scale access to photonic MPW runs [1]. First trial runs have also been made

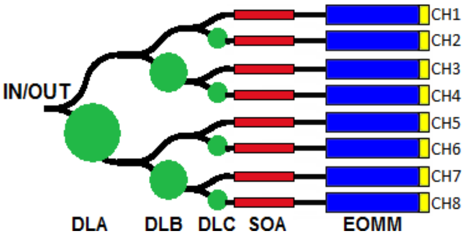

Figure 1: Schematic of the integrated optical serializer.

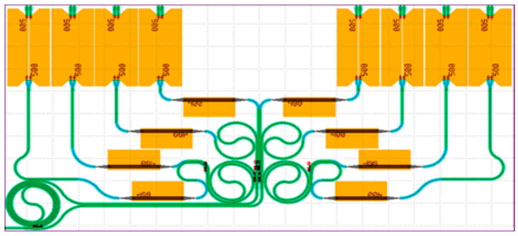

Figure 2: Mask layout of the serializer circuit.

at Oclaro in Caswell (UK) and at the Heinrich Hertz Institute in Berlin (Germany), within the framework of EuroPIC and the Dutch smartmix project Memphis.
In this paper we present the design and first experimental results of an integrated optical serializer, which is one of the ten pilot applications of the EuroPIC project. The chip has been fabricated in a Memphis-MPW run at Oclaro.

Chip design and mask layout

The integrated optical serializer finds its application as a readout unit for a large-scale physics experiment. The specification is based on the requirements imposed on the readout system for KM3NeT, a European collaboration that builds a cubic-kilometer-sized neutrino detector at the bottom of the Mediterranean Sea, 100 km off the shore. A basic module of the KM3NeT is a glass sphere containing 31 photomultiplier tubes that detect Čerenkov radiation from secondary particles generated by a neutrino interaction. The digitized signals have to be read out with a frequency of 1 GHz. We proposed to design a $32 \div 1$ serializer, of which the concept is described in [2]. In this work we focus on the $8 \div 1$ serializer chip, designed as a proof-of-concept circuit.
Optical serialization, or optical time domain multiplexing (OTDM), can be done by means of various methods [3, 4]. We use and implement a method that employs optical delay lines (DLs). The schematic of the circuit is shown in Figure 1. The input signal, a 1 Gb/s optical pulse train, is distributed among eight waveguides, that each have a specific length which delays the signal in each branch. We have applied a staged delay network, so that after each power splitter one of the outputs is delayed and the other is not. SOAs are used to compensate the losses introduced by circuit elements, propagation losses in the waveguides and splitting losses as the input signal is distributed among eight channels. The gain of each of the amplifiers can be tuned to obtain power balance among all of the channels. In each of them there is a different propagation length so that different attenuation as well. After the distribution the pulses are on-off modulated in Michelson modulators. Each modulator makes use of a multimode interference (MMI) power splitter, an electro-optic phase shifters and two MMI reflectors to build a Michelson interferometer. Figure 2 shows the mask layout of the designed circuit, measuring 2×4 mm^2.

Characterization results

The schematic of the characterization setup is shown in Figure 3. We used either a tunable laser diode or a femtosecond laser with a pulse width of 150 fs and 80 MHz repetition rate as light source. A polarization controller and a polarizing beam splitter were used to launch only the fundamental TE mode in the circuit. The optical signal is coupled to

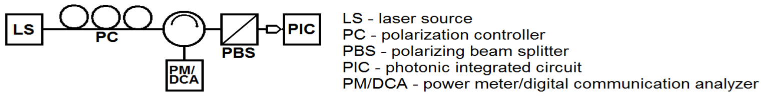

Figure 3: Schematic of the measurement setup.

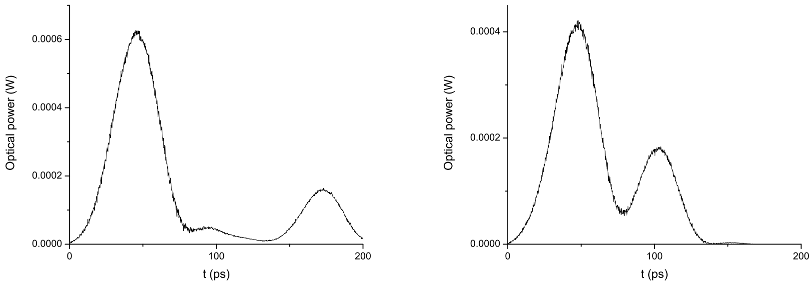

Figure 4: Time trace for the 5131 µm delay line (left) and 2211.9 µm delay line (right).

the chip with a tapered fiber. The outgoing signal was measured with a power meter or digital communication analyzer (DCA).

To determine the delay caused by the delay lines a pulsed signal was coupled to test structures. The output signal was measured in DCA. These are Michelson interferometers, with a spiral delay line in one of the branches. Figure 4 shows time traces for the two of such structures with the physical length of the line 5131.8 µm and 2211.9 µm, respectively. The broadening of the 150 fs laser pulse is due to the 30 GHz bandwidth of the DCA. The measured delays, 126.5 ps and 55 ps, are close to their designed values, which were 126.3 ps and 54.5 ps, respectively.

Transmission of an electro-optical Michelson modulator has been measured by launching a continuous wave laser signal and detection of the output power in a power meter. The arms of the modulator have been voltage driven. Figure 5 shows simulated and measured characteristics. In principle this is a fully symmetric structure, so that modulation of each of the arms independently should give the same transmission, as it is for the simulated curve. However, the measurement results show that there is an asymmetry in the characteristic. The figure presents two curves, when one of the arms is voltage driven and the other is grounded. We believe that the asymmetry is caused by unwanted excitation of higher order modes, resulting in an asymmetric power split between the modulator arms. The measured extinction ratio is 23 dB and 14 dB, depending on which of the two arms is driven, and is lower than simulated 29 dB. In the simulation the loss dependence on the driving voltage was underestimated, as the exact coefficients were unknown. The

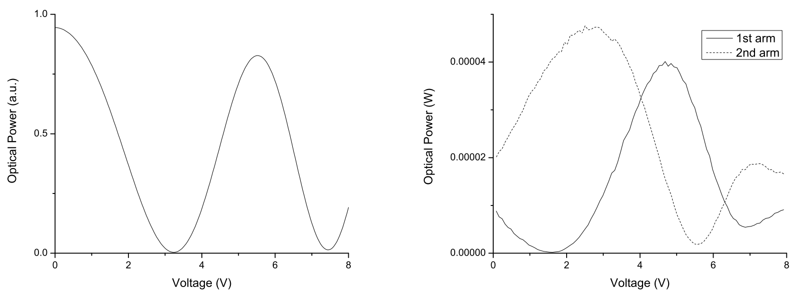

Figure 5: Simulated (left) and measured (right) modulator transmission characteristics.

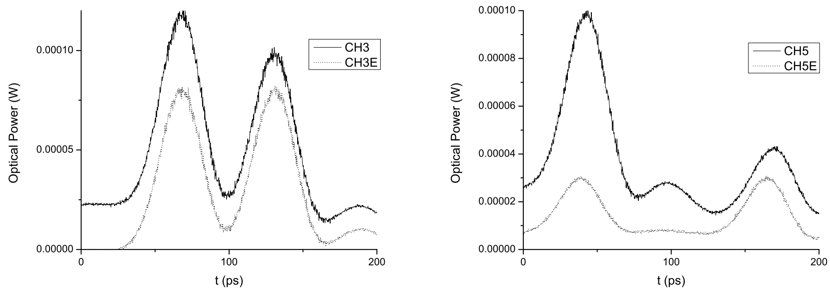

Figure 6: Time traces for channels 1 and 3 (left) and channels 1 and 5 (right) in the on-state.

measurement results show rise of the absorption with increasing voltage. It is worth to mention, that such a structure can be operated in a push-pull mode, so that one of the arms would be biased to shift the maximum transmission point to 0 V and thus increase the extinction ratio. The modulation voltage (V_π) is 3.0 V and 2.8 V for the two arms, slightly smaller than the simulated value of 3.3 V. This is a result of the shift of maximum transmission point and nonlinear dependence of the phase change on the driving voltage. Time domain characteristics, to determine the delay of the $8 \div 1$ serializer channels, have been measured by launching the pulsed laser signal to the circuit and detection of the serialized output pulses in the DCA. The SOAs of two channels have been simultaneously powered, so that the light in the other channels was absorbed completely in their SOAs. Figure 6 shows time traces while supplying the SOA in the first, non-delayed channel, and in channels 3 and 5, respectively. The measured delays are close to their designed values, 62.5 ps (CH3) and 125 ps (CH5). However, exact determination of the delay is limited due to the broadening of the pulses. In each case two measurements were undertaken. In the first (e.g. CH3) both operative SOAs have the same gain, whilst in the second (e.g. CH3E) the SOAs are operated to equalise the output channel responses. This shows that power balance between the channels is feasible.

Summary and conclusions

We designed an $8 \div 1$ optical serializer which was fabricated in an MPW run. We have observed serialization of the input signal and shown the possibility of power equalization among the channels. The modulator shows a good extinction of 20 dB. The first experimental results are promising for application of this concept in data readout systems.

The research leading to these results has received funding from the Dutch smartmix project Memphis and from the European Community's Seventh Framework Programme FP7/2007-2013 under grant agreement NMP 228839 EuroPIC.

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