Post-processing of a polarization converter for integrated polarization independent SOA[1]

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We report the post-processing of a passive polarisation converter (PC) in a photonic integrated circuit that is realized in a Multi_Project Wafer run at Oclaro. The chip contains structures for testing the PC in a polarization independent SOA configuration. Photo-resist is used to protect the existing devices, and a photo-lithography step defines the PC processing area. The device is made using wet etching to define the PC sloped sidewall, and EBL to define the PC waveguide. The measurement results show that the polarization dependence of the SOA reduced from 14 dB to 3 dB with the PC insertion.

Introduction

The design of photonic integrated circuits (PICs) is moving forward with the development of generic fabrication platforms, in which the most frequently used basic building blocks (BBs) are integrated in a circuit using a standardized process [1]. However, such a generic approach does not readily lend itself to include experimental BBs. The possibility to post-process devices in a PIC gives to the user the opportunity to test these experimental BBs in a circuit that contains validated structures. One such experimental BB is a polarization converter (PC). The PC is an essential BB in all the polarization handling devices such as polarization-scramblers, -splitters and -controllers, and furthermore it can be used to realize polarization independent devices. In this paper we describe the post-processing of a PC in a PIC fabricated by Oclaro. The chip design contains structures to test the PC in a polarization independent SOA (PI-SOA) configuration; tapered waveguides allow the connection between the test structures and the PC. In the first section we will explain briefly how the PC works and how it can be tested in a PI-SOA configuration. Next, we will describe the simulations performed to optimize the tapered waveguide connections. Then we will go through the post-processing steps. The last section is dedicated to the measurement results.

Polarization independent SOAs

A single section passive PC is an optical waveguide with a sloped cladding (Figure 1) connected to straight input-output waveguides. The PC waveguide geometry should be such that it can support the two modes M_1 and M_2, +45° and -45° rotated with respect to the TE vector. After equal excitation of the two modes by an input TE mode, and propagation along a half beat length $L_{PC} = \pi/(\beta_1 - \beta_2)$ the two modes recombine into

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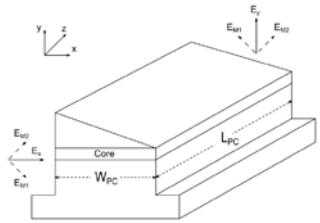

Figure 1: single section passive PC with sloped cladding.

the TM mode in the straight output waveguide [2]. Here β_n is the propagation constant of the mode M_n. The PC shape has been optimized for the Oclaro layer-stack. Details about the performance and tolerance analysis will be presented in a future paper [3]. We can obtain a PI-SOA, by placing a passive PC between two identical SOAs. Figure 2 shows the circuit working principle with a PC that gives a full conversion from TE to TM and vice versa ($C = P_{out}^{converted} / P_{out}^{total} = 1$). The output power in the case of a TE and TM polarized mode is shown as well, with $G(TE)$ and $G(TM)$ the gain of the SOA in the TE and TM case. Thus, by using a full conversion PC, this circuit gives a signal amplification independent from the input polarization (i.e., assuming that the SOAs are not in saturation). It can happen that $C \neq 1$. In this case, when the input mode is TE, the output power is $P_{out} = CP_{in}G(TE)G(TM) + (1-C)G(TE)^2$; if the input mode is TM, the output power is $P_{out} = CP_{in}G(TE)G(TM) + (1-C)G(TM)^2$. Thus, the output power depends on the input polarization. We use this circuit as test structure for our polarization converter.

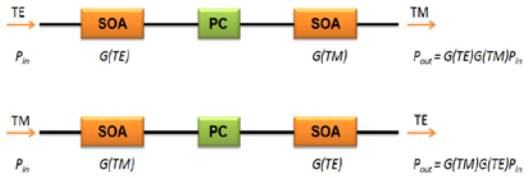

Figure 2: PI- SOA working principle.

Taper connections optimization

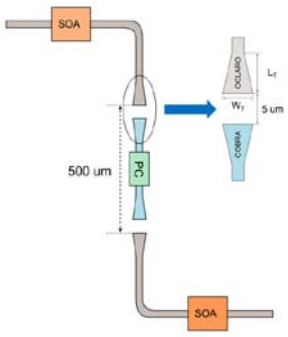

Figure 3: PI-SOA test structure and OCLARO-COBRA taper connection.

Figure 3 shows a schematic of a PI-SOA test structure together with the PC. The SOAs are defined in a direction perpendicular to the major flat, whilst the PC is defined in a direction parallel to the major flat, in order to obtain the sloped cladding by wet etching. The tapers allow the connection between the PC (post-processed at COBRA) and the rest of the circuit (processed by Oclaro). A 5 μm distance between the tapers is kept in order to process the PC with tapered input-output waveguides, using a separable technology process. The choice of the taper length L_T and width W_T is a compromise between performances and the aim to have a short device. The performances are evaluated in terms of coupling coefficient $k = P_{out} / P_{in}$. A pair of tapers, both 5 μm wide and 100 μm wide, give a $k = 0.95$. Since in the PI-SOA test structure the PC is connected by 2 pair of coupled tapers, $k = 0.90$; thus, the device has 0.5 dB extra losses due to the taper connections. We left a 500 μm space in between the Oclaro tapers to safely process the PC together with the COBRA input-output tapered waveguides.

Post-processing

The PC post-processing consists of two sequential processes: the Oclaro chip protection and the PC processing. The chip is protected with 400 nm of silicon nitride and with photo-resist. The nitride deposition is used later on as etching mask. The Oclaro circuit

is covered by spinning photo-resist AZ 4533 for 30 sec at 2500 RPM; the time and the speed of the spinning define the thickness of the photo-resist on top of the Oclaro structures. The photo-resist is then soft baked for 20 min at 95°C. A photolithography mask is used to open the areas for the PC processing. After the exposure, the photo-resist is developed using AZ-developer diluted 1:1 ratio in H_2O for 2 min and 30 sec. The last step is the photo-resist hard baking. The temperature is ramped from room temperature to avoid strain in the photo-resist, which causes cracks. At 200°C the photo-resist is baked for 20 min (Figure 4). The chip is then ready for the PC processing. The 400 nm nitride mask layer is already underneath the photo-resist. First, a O_2 plasma is applied to promote the adhesion between the EBL resist (ZEP) layer and the nitride layer; afterwards, the ZEP is spun on the chip. The ZEP layer remains quite uniform from the middle of the opened areas (around 350 nm thick) to 5 μm away from the Oclaro tapers (400 nm); therefore we can choose the same EBL dose factor everywhere to expose the structures. The PC is processed in two EBL exposures: the first one defines a rectangular area used to etch the slope in the cladding with HCl. The second EBL step defines the PC waveguide together with input and output tapered waveguides. The straight sidewalls in this case are obtained by RIE etching. However, the post-processed structures show a guiding layer undercut. A possible reason is that during the wet etching (HCl etching or cleaning steps) the presence of light influences the etch rate. This is known as the photo-electrochemical effect (PEC) and it can be enhanced by the presence of the back metal contact. Further experiments will be performed to verify this hypothesis. Figure 5 shows the protected Oclaro taper and the COBRA taper with the guiding layer undercut on the real chip, and the post processed PC on a dummy sample.

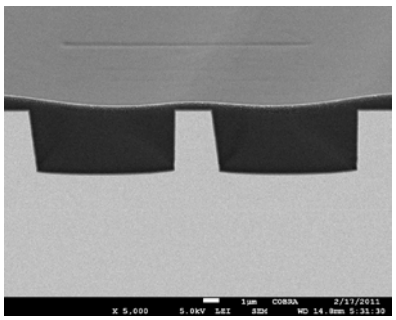

Figure 4: Oclaro taper cross-section covered with hard baked photo-resist (dummy sample).

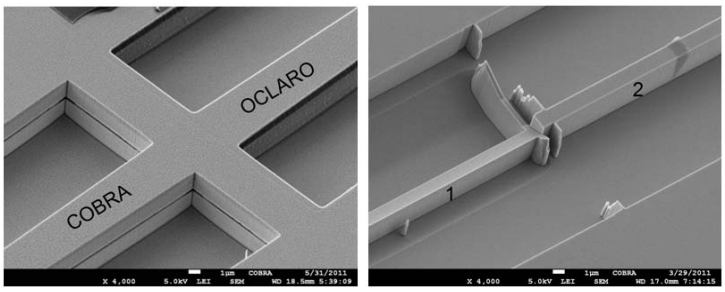

Figure 5: protected Oclaro taper and post-processed COBRA taper with guiding layer undercut (left); PC (1) with input waveguide (2) on dummy sample (right).

Measurements

The measurement setup is shown in Figure 6. The output fiber of a tunable laser, working at $\lambda = 1550nm$, is connected to a polarization controller. The polarization controller is used to minimize the output power $P_{out}^{\min}$ and then to maximize the output power $P_{out}^{\max}$. Afterwards we calculate $P_{diff} = P_{out}^{\max} - P_{out}^{\min}$ for two test structures: one with the PC (SOAs_PC) and one without

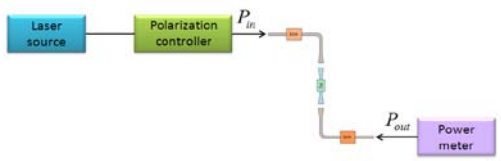

Figure 6: Polarization independent SOAs measurement setup.

PC (SOAs_noPC). In SOAs_noPC the PC is replaced with a deep etched passive waveguide 1.5 μm wide. The measurement results (Table 1) show that P_{diff} is smaller if the PC is present. The losses are high due to the guiding layer undercut.

	SOAs length	Drive current I	P_{in}	$P_{out}^{\max}$	$P_{out}^{\min}$	P_{diff}
SOAs_PC	500 μm	35 mA	5 dBm	-16 dBm	-19 dBm	3 dB
SOAs_noPC	300 μm	25 mA	0 dBm	-2 dBm	-16 dBm	14 dB

Table 1: Measurements results for the polarization independent SOA.

We also measured the losses in an Oclaro passive test structure without taper connections (Bends _Oclaro, Figure 7(a)) and then we compared the result with two passive test structures with taper connections. The first one is entirely made by Oclaro (Bends_tapers_Oclaro, Figure 7(b)); in the second one the central tapered waveguide has been post-processed at COBRA (Bends_tapers_COBRA, Figure 7(c)). The comparison between Bends _Oclaro and Bends_tapers_Oclaro shows that the taper connections introduce 0.5 dB losses (Table 2) which confirms the simulation result. Bends_tapers_COBRA has another 0.5 dB extra losses probably introduced by the guiding layer undercut.

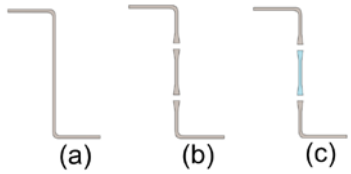

Figure 7: Bends _Oclaro (a); Bends_tapers_Oclaro (b); Bends_tapers_COBRA (c).

	P_{in}	P_{out}
Bends _Oclaro	0 dBm	-5.3 dBm
Bends_tapers_Oclaro	0 dBm	-5.8 dBm
Bends_tapers_COBRA	0 dBm	-6.3 dBm

Table 2: Measurement results for the taper connection losses.

Conclusions

A PC has been post-processed on an Oclaro chip containing test structures for polarization independent SOAs. The Oclaro-COBRA connection is realized trough tapers which give 0.5 dB extra losses. During the post-processing the Oclaro structures are completely protected; however a guiding layer undercut of the post-processed structures occurred. Further experiments will be done to solve this problem. Measurement results show that the polarization dependence of two SOA's in series reduced from 14 dB to 3 dB with the PC in-between, indicating the presence of a sizeable polarization conversion.

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