Bridging more than 100µm Step by Thick Photoresist Slope for 3D Chip Integration

P. Duan, O. Raz, B. E. Smalbrugge, E.J. Geluk, T. de Vries, H.J.S Dorren

Eindhoven University of Technology, COBRA, Den Dolech 2, 5600MB, Eindhoven

Interconnect density is gradually becoming a serious problem in computer systems. Three-dimensional(3D) device stacking is a promising approach to increase density and scalability. We propose a new way to bridge big steps between two stacked chips when Through-Silicon-Via(TSV) is not applicable. Our approach uses an ultra-thick photoresist layer to realize a smooth slope between two different height surfaces (such as 150 µm). The key processes developed are multilayer spinning and photoresist reflow. The step height is covered by electrical-plating for metallization and connection. Compared with wire bonding, this new strategy is fabricated on wafer scale and smaller inductance is introduced.

1. Why Need 3D Structure for optical interconnect?

Interconnect density is a critical limitation for computer performance improvement nowadays. Compared with metal wires, optical interconnect link exhibit inherent advantages for transferring signals from one place to another. Owing to photons lack of electrical charge, transmission loss is small and independent of date rate[1]. Optics can certainly avoid density limitations encountered in electrical systems, however, if we only use the perimeter of the chip to couple light into single mode fibers, there will not be enough space to communicate[2]. The required bandwidth demands the whole surface of the chip for transmitting, as the area scales quadratically with the chip's size allowing for an estimated 50 Tb/s for a chip measuring 310 mm^2 [3].
Closely stacking opto-electrical dies onto the top surface of a CMOS chip can maximize high speed interconnect performance and save footprint. Among all the stacking technologies, Through- silicon-via(TSV) is the most efficient 3D stacking approach, but it can only be used for thin silicon dies stack. 850nm opto-electrial dies widely used in the optical interconnect are based on GaAs, neither GaAs substrate nor silicon CMOS substrate is transparent at 850nm. IBM recently developed a novel optical transceiver Optochip, with physically drilled holes through CMOS for light path after flip chip attachment[4]. However, to realize holes in this special CMOS IC, approximately 20 RIE steps were required to etch through the film stack to expose the silicon wafer. Another demonstration is using wire bonding to connect opto-electrical device and CMOS[5]. The opto-electrical die was thinned down to 25µm before integration, which makes the opto-electrical device very fragile.

2. 3D stacking design

Our approach is based on stacking normal opto-electrical dies directly on the commercial CMOS drivers without grinding opto-electrical dies or drilling hole in the CMOS, and furthermore exploiting a simple and cheap solution to connect opto-electrical dies and CMOS drivers on a wafer scale. Inspired by the usage of thick photoresist in MEMS[6], our proposal is to form a smooth photoresist bridge between opto-electrical dies and CMOS driver underneath. Then a metallization layer is added on top of the phtoresist bridge by electrical plating, as shown in Figure 1.

There are two ways to realize a smooth photoresist slope. First method is using Grayscale lithography, which can be obtained by high energy beam sensitive glass as optical mask or utilizing projection lithography to introduce diffraction patterns. Second approach is based on the softening character of non-crosslink photoresist. Developed photoresist structure changes shape when samples are heated at or above softening point. In general, first approach is more complex, expensive and time consuming. We choose the second approach because it is much simpler, cheap, and because the size of our target pattern is big (contact pads on opto-electrical dies and drivers are at least 60μm).

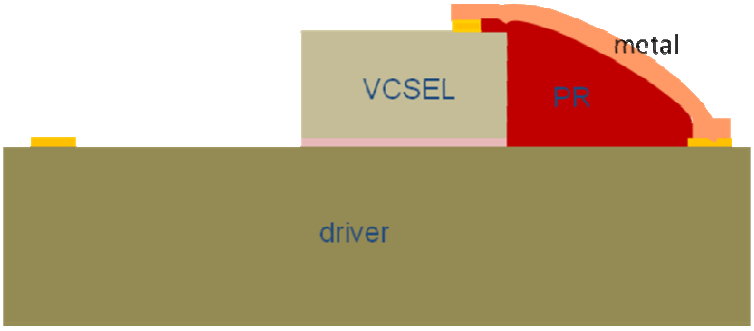

Figure 1 schematic demonstration of the bridge between VCSEL and CMOS driver

3. Fabrication and results

The key process we needed to develop is a smooth photoresist bridge from top opto-electrical dies to CMOS surface. The step height is approx.150 μm. Thick positive photoresist is highly viscous, it has better cover ability than thin photoresist, and also no cross link. So it is suitable for our purpose.

Firstly, we try to find right parameters to realize excellent edge cover ability. A 1000μm long, 250μm wide, 150μm thick dummy silicon die was glued to silicon chip to simulate opto-electrical dies stacking on the CMOS. Because the shape of samples is not circular, it is difficult to remove edge bead after coating. To lower the photoresist edge bead effect, we use multilayer coating by high speed spinning instead of low and short spinning. From Figure 2, we can see this multilayer coating strategy gives very good lithography results.

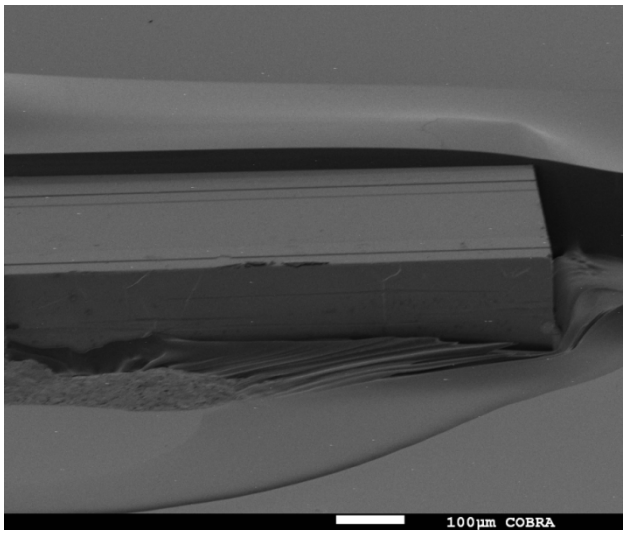

Figure 2.SEM image showing the coverability properties of the PR used on a dummy silicon on silicon chip

Secondly, we needed to verify that we can obtain the required resolution. Considering the fact that the distance between contact pads of opto-electrical dies are 30µm, the resolution of the ultra-thick photoresist layers should be better than 30µm. From the SEM picture in Figure 3, we can see the patterns are clear and pattern bottom open distance is the same as the mask (i.e. 20µm).

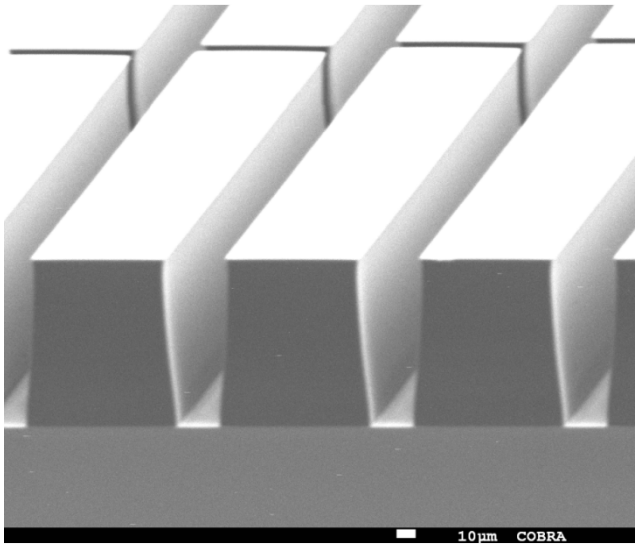

Figure 3. SEM image showing the obtainable resolution with aspect ratio=4:1

Thirdly, the reflow performance had to be tested. The reflow process is not only used for the bridge profile, but also enhance the adhesion between photoresist and substrate. To make a smooth slope of photoresist sidewall, developed patterns on samples are reshaped themselves on the hotplate which is above softening point. After reflow, the pattern cross section is shown in Figure 4. The sidewalls of the photoresist pattern are very smooth now with a typical angle of 30 °, which can be perfectly covered by metal evaporation or sputtering in the following process.

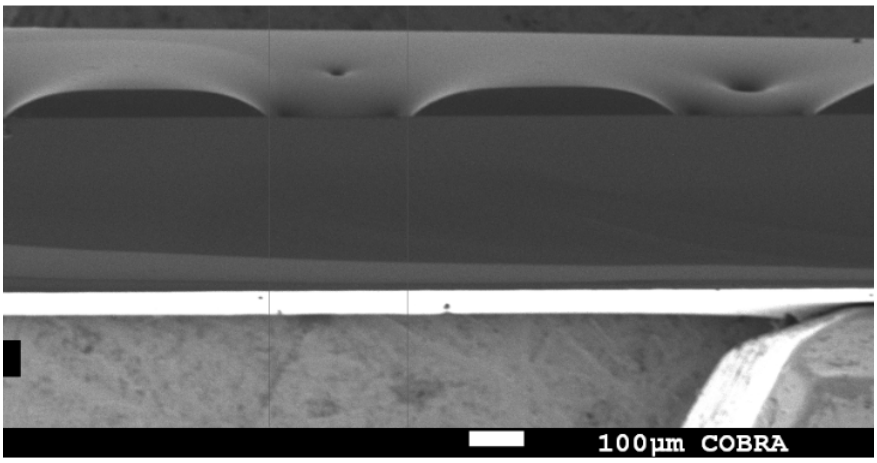

Figure 4. SEM image showing the photo resist profile after reflow

Finally, multilayer photoresist have been spun on the real device. Since only separate CMOS drivers are on the market, for processing convenience, a CMOS driver is glued on a silicon quarter by indium soldering, which guarantee devices can be removed after processing. After CMOS chip is fixed, we stacked an opto-electronic device on the right place on the CMOS driver. Now, there are two big steps on the silicon substrate: from silicon carrier to driver and from driver to opto-electrical dies. Same lithography and

reflow condition are used as before, the patterns on the different topography are shown in the Figure 5. Both patterns on the opto-electrical dies(highest surface) and driver(second stage) are clear and has smooth slope around patterns.

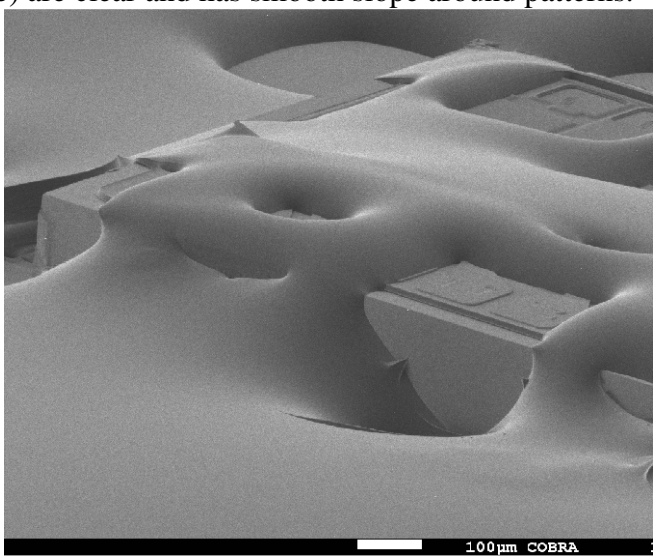

Figure 5 resulting photoresist bridge on the stacked sample

4. Conclusion and Future Work

A wafer scale process is demonstrated for connecting two quite different height surface for three dimension integration technology. It can be widely used as an efficient way to connect any fix paths. The significant advantage is that this process can be carried out on a wafer scale, making it much easier and cheaper than flip chip process. Since we used full-thickness opto-electrical dies, there is no reliability and handling issues which is related with opto-electrical thinning.

In this paper, we only realized the critical part of our approach, which is to use thick photoresist to form the smooth bridge between two very different height pads. Further work is being carried out to demonstrate also the metallization steps needed.

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