Design and Characterization of Spot Size Converters for Integration in InP-based Photonic Integrated Circuits

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We report on design and measurement of a series of spot-size converters (SSCs) for adapting the optical mode size in an InP-based photonic integrated circuit. SSCs are designed to transfer the mode of a 0.6mm-thick high-contrast waveguide to that of a 3mm-thick low-contrast waveguide below the core layer using a vertical taper. Fabrication of the taper is compatible with the standard processing and coupling loss values below 1dB have been achieved. Based on the experimental results we have designed an improved structure which enables adiabatic vertical coupling for taper lengths below 1mm. The simulation results predict losses below 0.5dB.

Introduction

Spot Size Converters (SSCs) are important components for reducing the losses in coupling light from the narrow waveguides in InP-based Photonic ICs to fibres that carry much larger modes. In this paper we report results from a series of experiments for the integration of vertically tapered Spot-Size converters, as reported previously by HHI [1] and us [2], in the InP-based generic foundry platform technology that is developed in the European projects EuroPIC and PARADIGM [3]. The SSC fabrication process is highly compatible with our platform technology; we succeeded in integrating the SSCs by adding only a few non-critical steps to the generic integration process. Our experiments show that losses below 1 dB to a waveguide with a 3 µm spot are possible for tapers with a length of 1 mm. The SSCs can be fabricated in dense arrays, with a pitch down to 25 µm, which allows their use in an optical bus for connecting the PIC to a dielectric interposer chip, as shown in Figure 1.

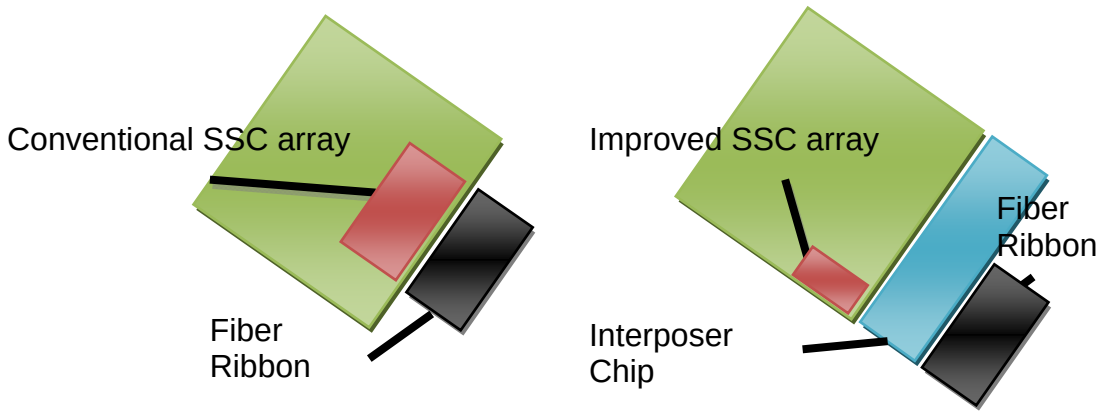

Figure 1: Schematic representation of a regular coupling configuration (left) and optical bus for a high number of ports, coupling effeciently to a passive interposer chip (right)

Concentrating all SSCs in a dense array has two advantages. The chip area required for the SSC array, which has a length in the order of 1 mm, becomes significantly smaller by positioning the SSCs at a pitch of 25 µm, instead of the usual 250 µm for fibre coupling. Further, the alignment requirements to the interposer chip apply to a much shorter region of the chip, so that the coupling is less sensitive to bow of the chip as a results of stress or strain in the waveguide layers. The interposer may be a simple expander that expands the pitch of the waveguides from 25 µm to the 250 µm of a fibre ribbon. However, it may also contain passive functionality, like low-loss delay lines or high-Q filters, thus forming a hybrid platform with the InP PIC.

SSC design

The presented design is an adaptation of [2], for making it compatible with our generic integration technology platform containing SOA's, High Speed Switches, Photo Detectors, AWGs, MMIs and other passive components [3]. Figure 2 shows a schematic picture of the Spot Size Converters. They transfer the mode from a 0.6 µm thick high-contrast waveguide layer in the PIC to a 3 µm thick low-contrast waveguide layer below it using a vertical taper. The low-contrast waveguide is formed by the index contrast between the highly doped n-type substrate and the 3 µm thick InP-layer between the waveguide layer and the substrate, which has been doped at a level of $5x10^{17}$ cm^{-3} in order to provide a sufficiently low resistance for the SOA's and the phase modulators that are integrated on top of this layer, while keeping the absorption loss sufficiently low. The mode size at the end of the taper is 3 µm, which matches well to an interposer realized in the low-loss Si_3N_4 technology that was recently reported by UCSB and LioniX [4]. A major advantage of the present design is that it is highly compatible with our generic process technology. The fabrication of the vertical tapers is done using a sliding raster mask technique, as described in [5].

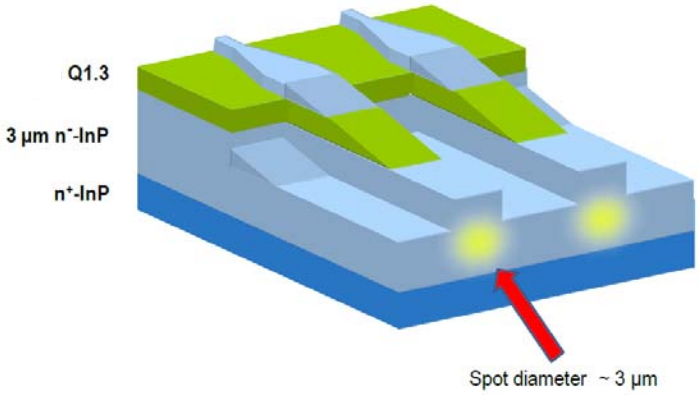

Figure 2: SSC array representation with a 3µm spot illuminating the facet of the doped low contrast waveguide

Experimental Results and Discussion

The characterization of the SSCs has been done using the Fabry-Perot measurement method. We have compared our measurements with simulation results using the two dimensional Beam Propagation Method implemented in the software Phoenix OptoDesigner and reducing the third dimension by means of the effective index method. We have simulated the above structure for different taper lengths. The dotted line in Fig, 4 shows the predicted taper loss as a function of the taper length for a lateral SSC

width of 10 µm. For the propagation losses in the taper region we found a value of 5 dB/cm. This is fairly high and probably caused by scattering loss at roughness of the top surface of the taper, which is created during the etching process that transfers the taper from the resist to the InGaAsP layer. We expect that this value can be reduced by further optimization of the etching process. The propagation loss of 5 dB/cm is indicated by the solid line in Fig.3. The dashed line gives the sum of the taper and the propagation loss. It is seen from Fig.3 that we achieved a very good agreement between the predicted and the measured results. This is especially the case for smaller ramps, as the absorption contributes less to the overall losses. For lengths above 1mm we clearly see that the total losses are dominated by the scattering losses. Best results that we achieved are below 1 dB, for tapers with a length of 1200 µm. By optimizing the etching process for reduced surface roughness we expect to be able to reduce the losses further to 0.5 dB.

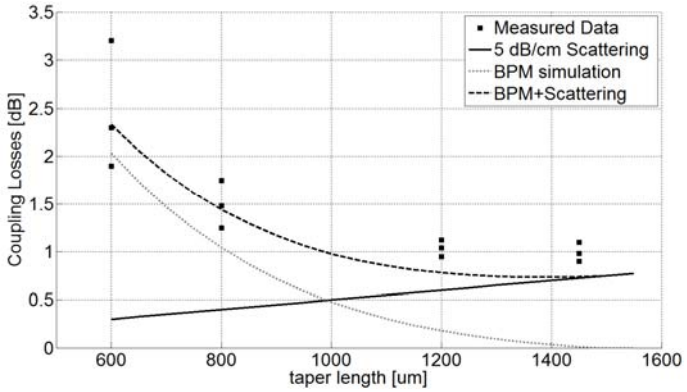

Figure 3: BPM simulation results for waveguide width of 10µm and measured SSCs taper losses

Redesign

The experiments above have confirmed that the vertical coupling needs at least a 1 mm long taper for high efficiencies. In order to improve the device, we included the concept of a diluted waveguide into our design. The basic idea is to displace the center of the mode in the low-contrast waveguide towards the upper taper to facilitate the transition. Therefore we investigated the effect of three 30 nm thin quaternary layers placed inside the low-contrast waveguide. By changing the distance of the central layer from the substrate and the spacing between the central and the outer layers we were able to find a good compromise between enhanced taper coupling and low fiber-chip coupling loss. The structure is displayed in the figure below.

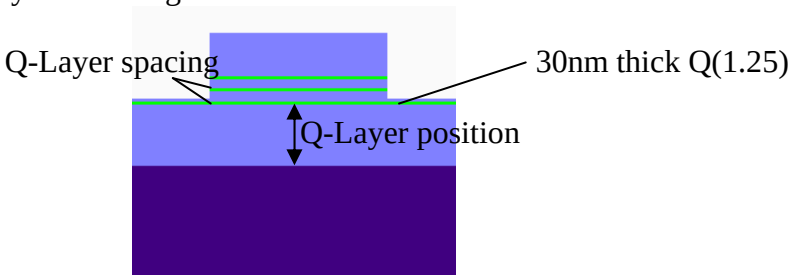

Figure 4: Cross-Section of the improved design, demonstrating the diluted low contrast waveguide

The calculations demonstrate that shifting the central Q-Layer position towards the taper improves the coupling. This is especially the case if the spacing is narrow, as this

will confine the center of the mode and facilitate the shift. For a promising configuration the length sweep in Fig.5 (right) shows that extremely low loss single slope tapers are predicted with a length of 550 µm and coupling losses around 0.4 db, which includes the experienced scattering losses from the reported experiment.

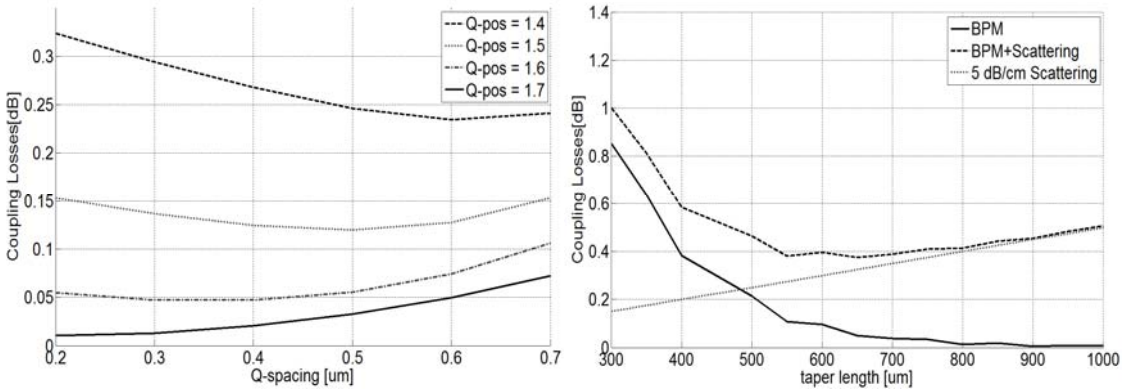

Figure 5: Influence of the Q-Layer central position and outer Q-Layer spacing on a taper length of 800µm (left) and BPM length sweep for the Q-position of 1.7µm with a spacing of 0.3µm (right)

Conclusion

We have designed and demonstrated a dense Spot Size Converter array for the realization of a compact optical bus in a generic platform technology for realization of InP-based Photonic ICs containing SOAs, high-speed phase modulators, detectors and passive components like AWGs and MMI-couplers. Conversion losses below 1 dB were demonstrated, in good agreement with simulations. Even lower losses can be obtained with an improved etching process and redesign. The proposed technology is highly compatible with the generic integration processes developed in the JePPIX platform (PARADIGM project). Only a few non-critical additional process steps are required for realization of the SSCs.

Acknowledgments

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