

A CMOS integrated opto-electronic receiver for automotive applications using 1 mm POF

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This paper presents the design and measurements of a fully integrated opto-electronic receiver operating at 650 nm, suitable for automotive POF data communication networks. The cost is minimized by applying butt coupling and integrating the PIN photodiode and the transimpedance amplifier in a 0.35 μm CMOS technology with a modified epitaxial layer. To cope with the large capacitance of the 1 mm photodiode and to improve the receiver's sensitivity, a fully differential structure with a dummy photodiode and regulated cascode buffer is proposed. Measurements show a sensitivity of -22.3 dBm at a BER of 10^{-9} for a stress MOST-pattern at a line rate of 334 Mb/s.

Introduction

Plastic optical fibers gain a lot of interest for automotive data communication networks as they offer many advantages, such as the insensitivity to electromagnetic interference, the relatively high bandwidth, the ease of handling and installation, low weight and a small cross section. The design of network components for automotive data communication is very challenging as it requires a high performance at very low cost in an automotive environment, which is characterized by a high temperature range (junction temperatures of -40 °C to 125 °C) and a large level of electromagnetic interference [1]. This paper presents a low-cost receiver with large-area photodiodes integrated in a CMOS process using a modified wafer with a 20 μm intrinsic layer. The large junction capacitance of 5 pF (+/- 25 %) complicates the receiver's design as it reduces the achievable bandwidth and sensitivity severely.

Design of the differential opto-electronic integrated receiver

Figure 1(a) depicts a simple block diagram of the realized receiver chip, existing of two identical integrated photodiodes, a differential current buffer (CB), a differential Transimpedance Amplifier (TIA) and an output buffer. A dummy photodiode, which is fully shielded from any incoming light, represents the parasitic PIN capacitance, in order to make the receiver as symmetric as possible. In this way, the receiver is immune to common mode noise, e.g. originating from the substrate and electromagnetic interference.

Highly sensitive front-illuminated NIP photodiodes, with a relatively small junction capacitance, are realized in 0.35 μm CMOS as follows (Figure 1(b)): a 20 μm thick, very low doped epitaxial layer is applied to the p+ substrate wafer, acting as the intrinsic layer of the PIN structure. The majority of the light passes the very low resistance cathode, realized by a thin, but very high n+ implementation at the top of the wafer. The p+ substrate is acting as a common anode, which is connected at the top of the wafer by means

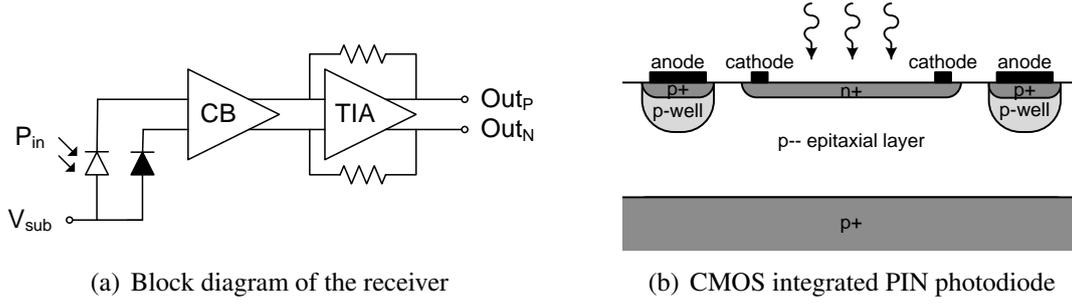


Figure 1: The opto-electronic integrated receiver.

of deep p-wells. In order to deplete the junction of the photodiode, an external reversed bias is applied to these anode contacts. The surrounding circuitry is put into deep floating n-wells, protected against the high reverse voltage. TCAD simulations of a 1 mm diameter photodiode, show a junction capacitance of 5 pF and a 3 dB cutoff frequency of 270 MHz for a 650 nm light source.

Expensive lenses and accurate alignment are avoided by applying butt coupling, thus significantly reducing the cost of the receiver. In order to achieve efficient coupling of the POF fiber, the diameter of the integrated photodiode should be chosen sufficiently large to capture most light, but not too large as the parasitic capacitance increases with the square of the diameter. The coupling efficiency, shown in Figure 2(a) for a misalignment of 150 μm , is given by:

$$CE = \begin{cases} \frac{D_{diode}^2}{D_{spot}^2} & D_{diode} \leq D_{spot} - 2d_{xy} \\ \frac{D_{diode}^2(\alpha_{diode} - \sin(\alpha_{diode})) + D_{spot}^2(\alpha_{spot} - \sin(\alpha_{spot}))}{2\pi D_{spot}^2} & D_{spot} - 2d_{xy} < D_{diode} < D_{spot} + 2d_{xy} \\ 1 & D_{diode} \geq D_{spot} + 2d_{xy} \end{cases}$$

$$\text{with } \alpha_{diode} = 2\arccos\left(\frac{d_{xy}^2 + D_{diode}^2 - D_{spot}^2}{4d_{xy}D_{diode}}\right) \text{ and } \alpha_{spot} = 2\arccos\left(\frac{d_{xy}^2 + D_{spot}^2 - D_{diode}^2}{4d_{xy}D_{spot}}\right)$$

with D_{spot} the fiber's diameter, D_{diode} the photodiode's diameter and d_{xy} the misalignment of the fibre to the photodetector. For a given bitrate, the sensitivity of the receiver - assuming ideal coupling - decreases with increasing input capacitance [3]. Figure 2(b) show the simulation results for the designed TIA for different photodiode diameters.

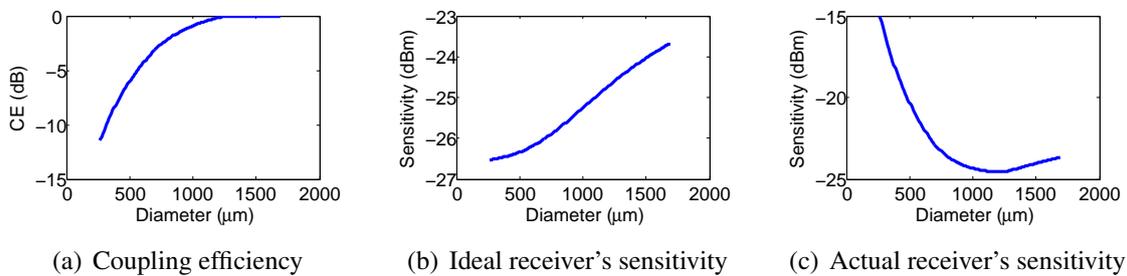


Figure 2: Defining the optimal photodiode diameter

The actual receiver's sensitivity, including the coupling loss of the POF fiber to the photodiode, is shown in Figure 2(c), resulting in an optimal photodiode diameter of around 1

mm. Note that the optimal photodiode is not always equal to the fiber's diameter. For a PCS fiber with a 200 μm diameter, the optimal diameter is larger than 400 μm assuming the same mechanical tolerances.

A current buffer is applied to decouple the large PIN parasitic capacitance from the band-

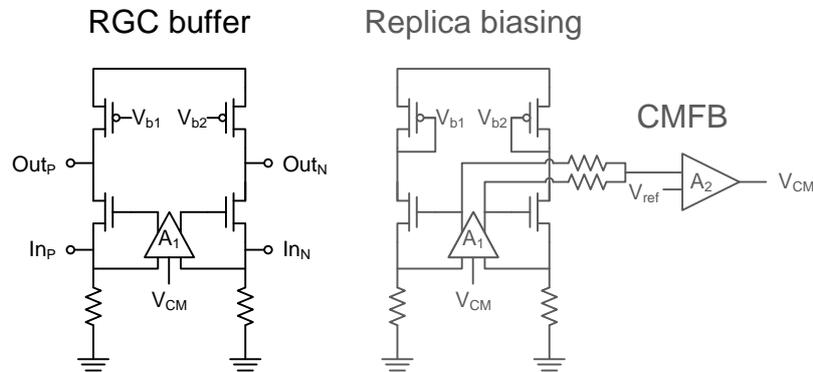


Figure 3: The current buffer

width determination, by reducing the input impedance and thus shifting the dominated pole towards the succeeding TIA. A current buffer can be realized by a common drain (CD) configuration, lowering the input impedance to $Z_{IN} = \frac{1}{gm}$ in stead of $Z_{IN} = \frac{R_F}{A_{TIA} + 1}$ for a conventional TIA. In order to circumvent the rather small gm/ID ratio of a CMOS process, the input impedance is further lowered by means of a regulated cascode buffer (RGC) ([3, 4]), as depicted in Figure 3. As one side of the CB is grounded, the resulting input impedance is equal to $Z_{IN} = \frac{1}{gm \cdot (A_1/2 + 1)}$.

A replica biasing circuit ensures that the current of the pmos current sources is equal to the biasing current through the common gate transistors. Thereby, the DC-current flowing towards the feedback resistance of the TIA is minimized, thus improving the increasing the TIA's linearity. Consequently, the stability of the DC operating points with temperature are improved. The common mode feedback (CMFB) in turn control pulls the voltage of the cathode of the PIN photodiode as high as possible.

The TIA's core amplifier is a conventional differential pair with passive loads, succeeded by source followers.

Experiments

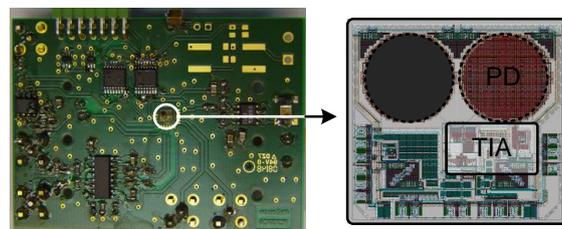


Figure 4: Test board and layout of the opto-electronic integrated PIN-TIA

The PIN-TIA chip is processed in the standard 0.35 μm CMOS technology of XFAB using a modified wafer. The chip occupies 2.7 mm x 2.6 mm, including test circuits. The

receiver's test board, including a naked die PIN-TIA chip and a commercial Limiting Amplifier (MA3645) is shown in Figure 4, together with the PIN-TIA's layout. Figure 5(a) depicts the test setup, used to perform sensitivity measurements. The parBERT generates a MOST pattern [5] at a line rate of 334 Mb/s in order to modulate the commercial laser diode (Firecomss EDL1000T) with an extinction ratio of 10 dB. Figure 5(b) depicts the measured BER performance, showing a sensitivity of -22.3 dBm for a BER of 10^{-9} . An external reverse bias of -7 V to fully deplete the junction was applied. Measuring the sensitivity over an environmental temperature range from -40 °C to 105 °C shows a variation of only 1.2 dB.

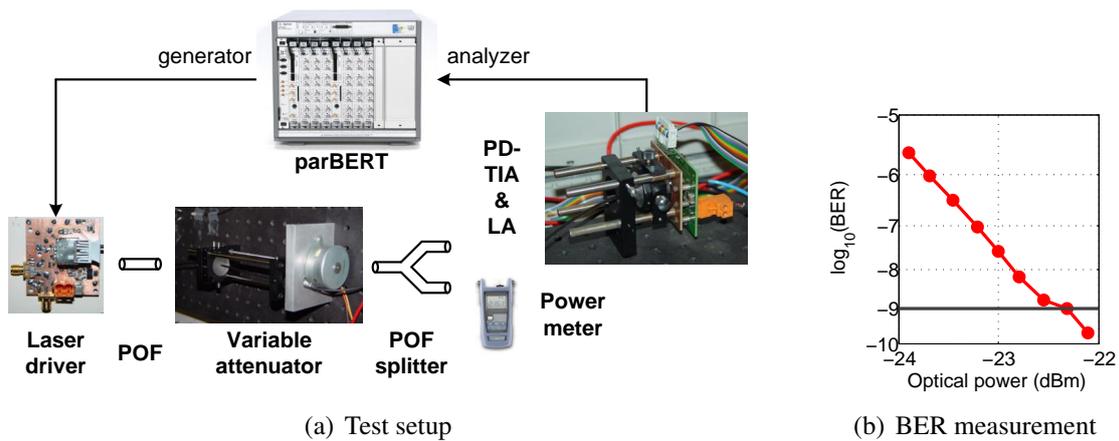


Figure 5: Experiments

Conclusion and Acknowledgement

A low-cost opto-electronic receiver have been designed for a butt coupled large core (1 mm) POF fiber. Therefore, the optimal photodiode diameter is derived, a very low doped 20 μm thick epitaxial layer is applied and an RGC buffer is placed in front of the TIA. Experiments show a sensitivity of -22.3 dBm at a BER of 10^{-9} for a stress MOST-pattern at a line rate of 334 Mb/s.

This work is supported by Melexis and by the Flemish Government under the IWT Grant 070193 "OptoCMOS". The authors also wish to thank Melexis and XFAB for the technical support, the collaboration and the chip fabrication.

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