A new zero-level package approach for receiver modules

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Compact integrated receiver modules are key building blocks for high bandwidth density interconnection links. Previously, a 3D stacked receiver module was fabricated by utilizing an ultra-thick photoresist ramp to form a wafer level package strategy. In this paper, we will demonstrate another integrated approach based on the same technology. Instead of stacking the photodiode array on the TIA/LA chip, we placed them side-by-side on a silicon carrier in very close proximity. The metallic connections between the photodiode pads and TIA/LA pads were realized using electrical plating after a photoresist bridge is created between the two components. Visual inspection using a SEM show that connecting metal stripes are uniform and of good quality.

Introduction

The performance of today's computer systems is limited by signal transport (data communication), rather than by the logic operation speed or memory capacity [1-4]. Although, traditional copper wires are improving their performance by exploiting advanced techniques, such as active copper cables [5], these advances will not satisfy future interconnect requirements of bandwidth density and bandwidth distance product, due to the inherent limitation of the electrical wires [2].

Optics has improved bandwidth distance product and bandwidth density and if implemented in a cost effective-manner, optics may bring substantial system performance improvements [2]. Parallel optical links are already widely used in today's supercomputers for chassis-to-chassis and rack-to-rack communications [4]. These optical interconnects continue support higher speed, smaller package size, lower energy per bit and lower cost. Especially for cost-sensitive data center application, one of the critical figure of merits has decreased from $100/Gbps in 2004 (VCSEL is around $10 per each die) [3] to today's $1/Gbps [2], and it needs to go below 10's of cents/Gbps [4] to support further penetration of this technology. In this paper, we will demonstrate a new zero-level package approach. This approach can allow for placing devices close to each other, without the need to accommodate requirements which normally exists in wire bonding technology [6]. It also processed at modest temperature, which is not the case for the flip chip [7]. Finally we show that with the same technology steps we can also improve coupling to fibers by making micro lenses on top of the O/E and E/O dies.

Fabrication

Previously, we have proposed a novel 3D stacking solution [8]. It can be used as an efficient way to connect any fix paths of two quite different height surfaces on a wafer scale process, such as integration of VCSEL array, photodiode array with its counterpart CMOS IC to form a 3D stacked transmitter and receiver array[9]. Recently, we explored a new package approach, which offers an effective way to connect devices on the same

carrier. The key step is to use the good topology cover ability and reflow character of ultra-thick photoresist, to form the photoresist bridge for plating process. This PR bridge can be deposited on all the metal connections between all the pads at once.
In the experiment, a 2-inch silicon quarter is utilized as a carrier since silicon has high thermal conductivity, which matches the thermal expansion of the CMOS IC chip and it is cheap. A 12-channel PD array and TIA/LA chip will be placed side by side on the carrier to form the receiver module. To speed up the pick and place process, 50nm silicon nitride are firstly deposited on silicon quarters, then using lithography and dry etching the placement spots of photodiode array and TIA array are defined. In this way, automatic pick and place machine can be used to put devices on the carrier through image recognition software. The photodiode array and TIA/LA array are successively placed on a dummy silicon quarter. After removing the redundant PR bonding layer, the sample is shown in Figure 1, the photodiode array is juxtaposed to a TIA/LA chip.

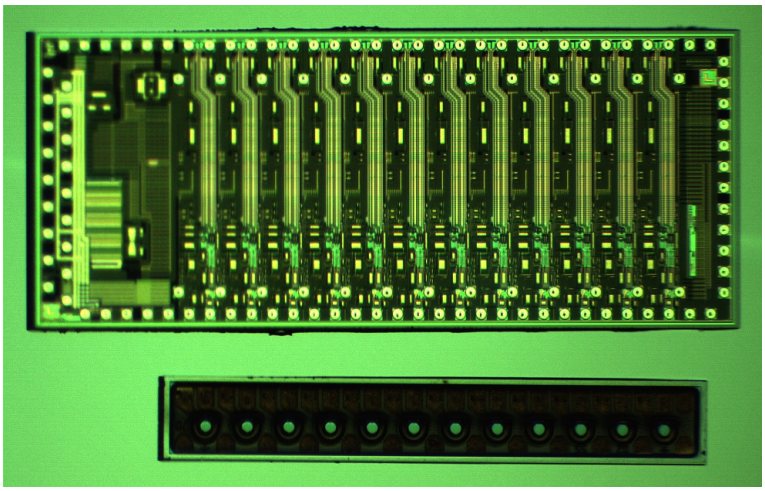

Fig. 1: 3D stacking model demonstration after placement

The photoresist pattern is obtained in the similar way as reported in [8]. After lithography, the chip is shown in Figure 2(a). You can see, the PR pattern covered the edge of TIA/LA chip as well as the edge of the photodiode array very well. In this process, we also introduced a cylinder pattern which fulfills two purposes. Firstly it provides protection to the sensitive area on the aperture of the photodiode array, shown in the Figure 2(b). Secondly it can be used as micro-lenses to help improve the coupling efficiency [9].

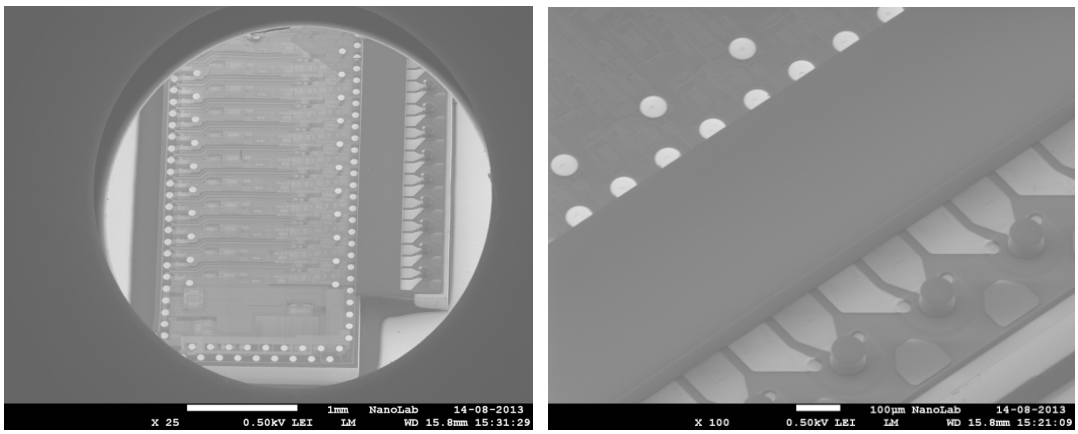

Fig. 2: (a) the sample outlook after lithography; (b) the zoom-in picture to show the photoresist cylinder pattern on the active area of photodiode array

The next step is to reflow the PR. As shown in the Figure 3, the photoresist ramp is smoothly formed between CMOS IC and photodiode array after the reflow step. The cylinder photoresist patterns turn under these conditions into semi-spheres due to the surface tension.

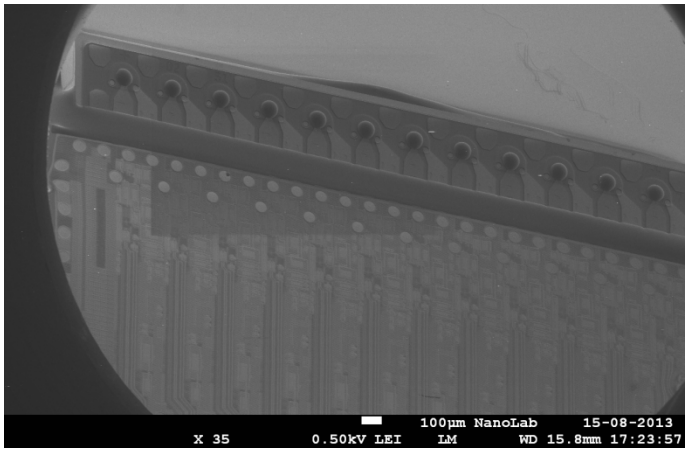

Fig. 3: the sample after reflow

After sputtering of a seed layer, we use lithography to define the plating area. Since the PD and the TIA/LA chip are placed side by side, the height between photodiode array surface and TIA/LA surface is decreased, so less overdevelop is needed in the process compared with previous approach [8], and much denser pitch can be realized in this way. As shown in the Figure 4, the opening rectangular pattern is formed on the seed layer, which will be plated with gold in the next step.

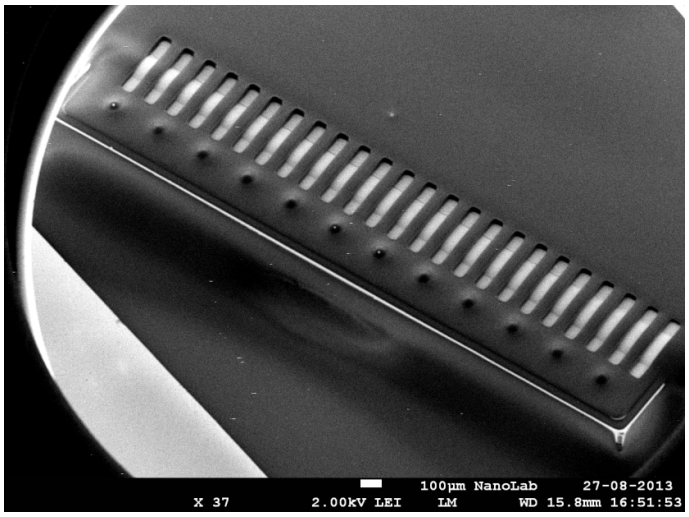

Fig. 4: the sample after lithography to define the plating area

The plating process determines the thickness of the metal paths. After plating, the photoresist and the seed layer are removed one by one. The chip looks like in Figure 5(a) after the process is complete. All 24 plated gold paths show good connections between photodiode pads and TIA/LA pads, and all the lenses are strongly attached onto the aperture of the photodiode array, as shown in the Figure 5(b). The resistance of each metal trace is negligible, the dark current and I-V curve of each photodiode remains the same as those for the original dies, and the photocurrent of each photodiode channels is double the number of the original photocurrent per each die at the same intensity flood light testing environment, thanks to the focusing of the lenses. In addition, you can also

see the metal paths are quite short, less than 200 µm when we pushed the photodiode array to almost touch the TIA/LA chip. Together with possibility to design the metal stripes to be impedance matched, this technique is very promising for higher data rate transmitter and receiver modules. Furthermore, the process itself is simpler due to the small height difference between each device on the carrier.

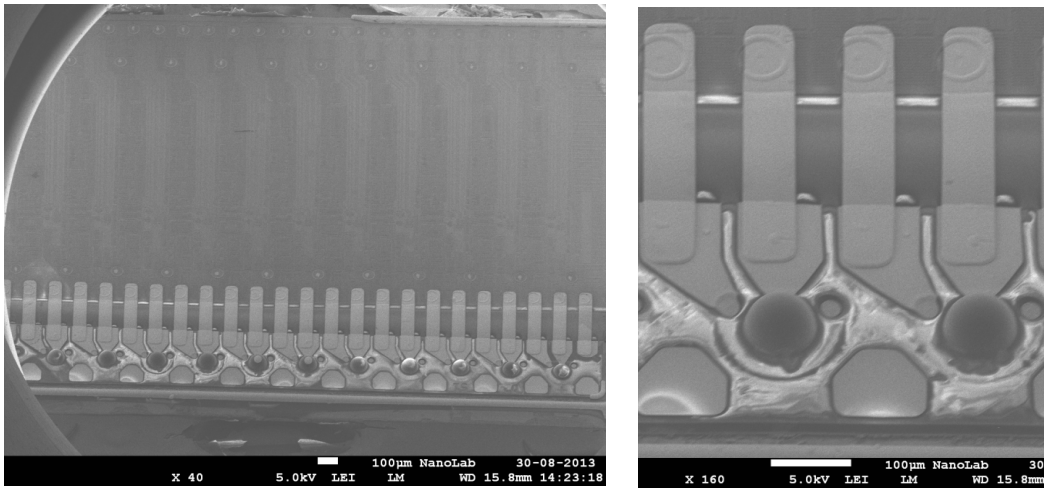

Fig. 5: (a) final shape of the side-by-side placed receiver chip, (b) the picture of micro-lenses and the plating metal paths

Conclusions

In this paper, a new integrated approach is demonstrated. Instead of stacking the photodiode array on the TIA/LA chip, we placed them side-by-side on a silicon carrier in close proximity. The primary test results show robust performance is achieved together and that the micro-lenses included in the fabrication process improve coupling. This new method can also be used for other high-speed, pressure-sensitive and temperature-sensitive devices interconnections and packaging challanges.

Acknowledgements

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