Dynamic Routing in a Resonant Switch Matrix

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Higher order ring resonators offer a possible avenue for broadband routing of optical signals. Recently we have reported broad bandwidth and high signal extinction in a 4×4 monolithically integrated optical switch matrix using fifth order resonators. In this paper we study the first dynamic multi-path routing experiments across a range of paths in the resonant switch matrix connecting two inputs to one output at a time. Further, we report the routing across a higher number of switching elements with modest losses, connecting combinations of ports for up to eight inputs and two outputs in the same monolithic optical switch matrix.

Introduction

High fabrication tolerance CMOS process combined with high confinement, low loss, Silicon on Insulator (SOI) waveguides has led to considerable and renewed research into micro-ring resonator technology. Optical switch architectures have been studied in some detail, primarily by placing single-order micro-rings switch elements at the intersections of multiple meandering waveguides to create modest connectivity 'optical router' elements [1,2]. The single order micro-ring is conceptually attractive but the inherent trade-off between the spectral-passband-width and the pass-band-to-stop-band signal extinction [3] compromises the switch scalability. Additionally, nanoscale fluctuations in waveguide dimensions lead to resonant wavelength fluctuations in the order of 1nm in nominally-identical ring resonators across a wafer [4,5] which is significant when compared to the narrow operating bandwidth. Simultaneous optimization of the passband width and switch extinction has been demonstrated in higher-order ring resonant elements though [6]. We have recently demonstrated 40Gbps routing across representative paths in a 4×4 switch matrix of higher order resonators [7]. In this work, we use this scalable crosspoint switch matrix to demonstrate dynamic multi-path routing for the first time in a large optical switch matrix with paths with up to eight elements in one row.

Circuit Fabrication

The optical switch matrix was fabricated on a $12\times12mm^2$ SOI chip diced from an ePIXfab multi-project wafer. Low-cross-sectional area $500\times220nm^2$, high-confinement silicon waveguides are used along with 1.2µm and 2µm upper and lower SiO_2 cladding layers. The input and output buses required for the optical crosspoint matrix run vertically and horizontally across the chip respectively and fifth order resonant switch elements are located at each intersection. Waveguide crossings are implemented with $32\times3\mu m^2$ MMI couplers to complete the formation of the matrix. Grating couplers optimised for TE polarisation are used in combination with horizontal tapers to couple light into each input and output. These are located at the bottom edge of photograph which is shown in Fig. 1.

On-off switching is realized by tuning the transfer function of each ring by means of a thermo-optically induced refractive index change. Micro-heaters are fabricated on top of the foundry-supplied SOI circuits. A metallisation comprising 100nm Ti, 20nm Pt and 300nm Au is evaporated and patterned to create the on-chip wiring and microheaters. The on-chip wiring is implemented with 18.5µm-wide tracks and the heater elements are constricted in width to 3µm. A selective Au etch is carried out for the micro-heater elements to increase their resistance to around 400 Ω. A polyimide layer is spun over the photonic circuit and the microheaters to provide protection against thermally-induced degradation. The bondpads and the grating couplers are re-opened at the end of the process for electrical and optical connections.

The microheater at each switch element is individually addressed. A common ground is used for the entire circuit and hence the fabricated m×n matrix has (m×n)+1 electrodes. Wire bonds leading off from the chip as shown in Fig.1, enable external electrical connectivity to each switch element. The chip is fixed to a water-cooled mount in order to maintain the chip at a constant temperature of 22 °C.

Fig. 1. Photograph of assembled circuit. Wire bonds leading to the left and right of the image are control lines. Wire bonds leading to the bottom edge are the common ground lines.

Results

A 10Gbps, 2^{31}-1 PRBS, on-off keyed optical signal is generated with a tunable laser tuned at 1551.35nm and a Mach-Zehnder modulator. The signal is split into two and input into two ports of the switch matrix. The output from the switch matrix is initially amplified by a low noise amplifier with an output optical signal to noise ratio (OSNR) of 30dB/0.1nm. A 0.9nm full-width at half maximum band pass filter (BPF) is used for noise rejection. The amplified output is fed into an optical receiver and viewed on a sampling oscilloscope as shown in Fig. 2.

Three fibers are used perform multi-path analysis: Two fibers are used as the input into the chip and with polarisation controllers put in place to optimise the input polarisation. The third connects the output to test equipment. All three fibres are separately aligned to minimise the fibre-chip coupling loss to 6dB per fiber.

Initial assessment of the switch elements is carried out by characterizing the error rates for the full range of paths. A selection of the paths tested are summarised in Table I. A

path independent power penalty is noted with the highest penalty being 0.7dB for the path from input 5 to output 2.

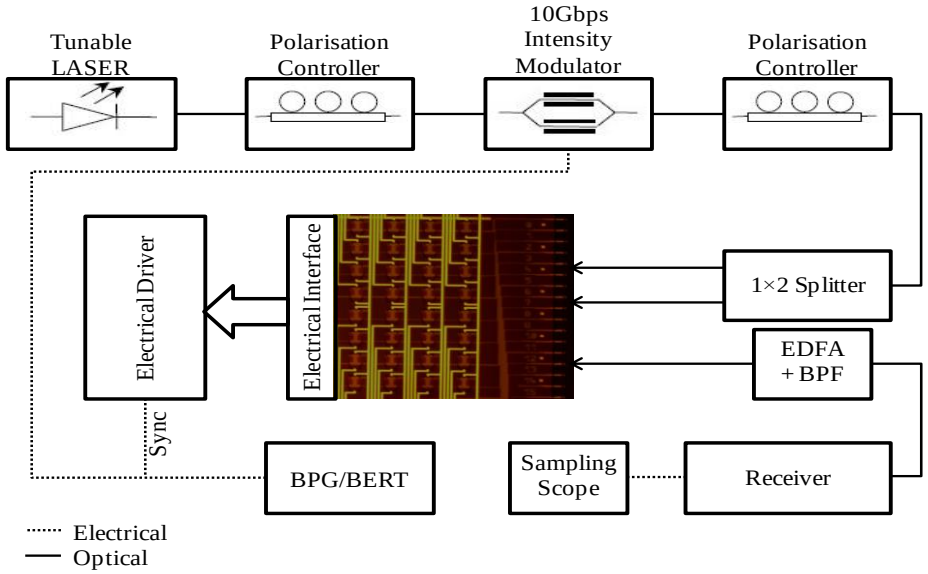

Fig. 2. Experimental arrangement for the study of dynamic multi-path routing.

Table I: Power penalty and bias voltage levels for selected paths through the optical switch matrix

Ring Element	"On" state bias (V)	"Off" state bias (V)	Power penalty in the "On" state (in dB)
8×2	3.14	7.44	0.3
7×2	3.47	6.93	0.5
6×2	2.84	7.21	0.6
5×2	5.22	8.71	0.7
8×1	0.00	6.71	0.3
6×1	2.22	7.15	0.5

Bias conditions are optimised individually and example values are included in Table I. Each micro-heater is actuated with one control voltage and this tunes all five resonators together for the fifth order switch element. The absolute values for the on and off state biases do vary between the switch elements and this highlights the requirement compensate for the nanometer scale fabrication variations and resonant wavelength registration errors across the optical switch matrix.

Dynamic routing is subsequently demonstrated by applying 750µs period square wave signals to two of the optical switch elements. Routing is performed from inputs 6 and 8 to output 2 and also from inputs 5 and 7 to output 2.

The time traces shown in Fig 3a and b show the output signals toggling from input 6 to 8 and input 5 to 7 to output 2 respectively. The vertical axis is fixed for each of the measurements to show modest levels of path dependant loss. Fig 3c and d show routing to output 1. Fig. 3a, b and c show a distinct difference in signal levels which correspond to the path dependant losses across the chip. The power levels in the guard bands is nearly zero which is consistent with the measured off state signal leakage of below 20dB.

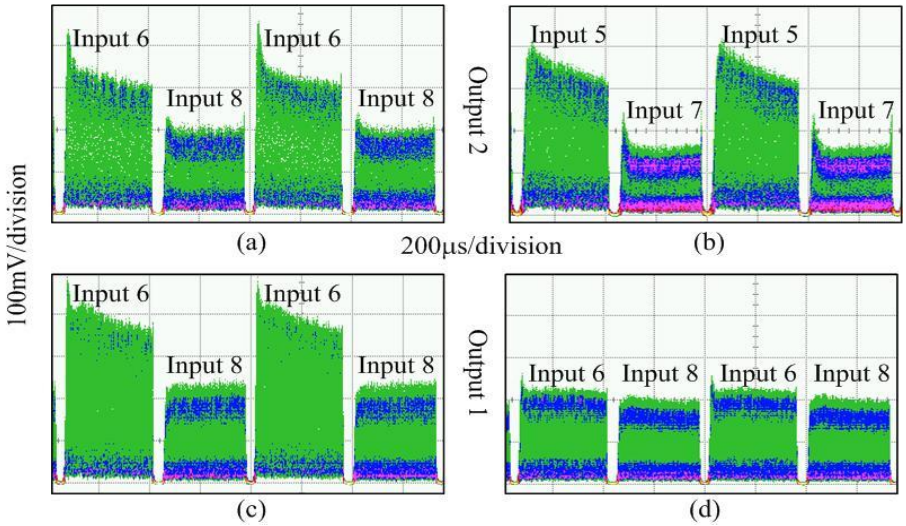

Fig. 3. Dynamic routing for 10Gb/s data for three combinations of inputs to outputs with (a-c) power equalized at the input to the optical switch matrix, and (d) power equalized at the output of the optical switch matrix through additional optimised losses on the input side.

There is a time-dependent power drop visible in Fig. 3a, b and c but this can be removed when the input power levels are adjusted to give equalized output levels as shown in Fig. 3d. The power excursions in Fig. 3a to 3c may be attributable to the carrier lifetime in the fibre amplifier.

Conclusions

We have successfully demonstrated signal routing at 10Gbps across multiple paths of a switch matrix with static power penalties below 0.7dB. The first demonstration of dynamic connection of multiple inputs to a single output is also carried out. This facilitates routing across a span of up to eight inputs and two columns, and the prospect of further scaling in microresonant switch matrices.

References

[1] A. Biberman, B.G. Lee, N. Sherwood-Droz, M. Lipson and K. Bergman, "Broadband Operation of Nanophotonic Router for Silicon Photonic Networks-on-Chip," IEEE Photon. Technol. Lett., vol. 22, no. 12, pp. 926-928, Jun. 2010.

[2] R. Ji, L. Yang, L. Zhang, Y. Tian, J. Ding, H. Chen, Y. Lu, P. Zhou, and W. Zhu, "Five-port optical router for photonic networks-on-chip," Opt. Express, vol. 19, no. 21, pp. 20258-20268, Oct. 2011.

[3] K.A. Williams, A. Rohit, M. Glick, "Resilience in optical ring-resonator switches," Opt. Express, vol. 19, no. 18, pp. 17232-17243, Aug. 2011.

[4] T. Barwicz et al., "Silicon photonics for compact, energy-efficient interconnects [Invited]," J. Opt. Netw., vol. 6, no. 1, pp. 63-73, Jan. 2007.

[5] S.K. Selvaraja, W. Bogaerts, P. Dumon, D.V. Thourhout and R. Baets, "Subnanometer Linewidth Uniformity in Silicon Nanophotonic Waveguide Devices Using CMOS Fabrication Technology," IEEE J. Select Topics Quantum Electron., vol. 16, no. 1, pp. 316-324, Jan. 2010.

[6] Y. Vlasov, M.J. Green and F. Xia, "High-throughput silicon nanophotonic wavelength-insensitive switch for on-chip optical networks," Nature Photon., vol. 2, no. 4, pp. 242-246, Apr. 2008.

[7] P. DasMahapatra, R. Stabile, A. Rohit and K.A. Williams, "40Gb/s data routing through a scalable 2D matrix of higher order ring resonator switches", IEEE Electronics Letters (Accepted).