A Cost-effective PCB-based Optical Transmitter for Optical Interconnect Using Broadside Coupled Differential Pair

T. Li, R. Stabile and O. Raz

Benelux COBRA Research Institute, Eindhoven University of Technology, The Netherlands, E-mail: T.Li@tue.nl

We use the broadside coupled differential pair structure on printed circuit board (PCB) to achieve a high-speed optical transmitter. Compared to edge coupled differential pair, this structure makes it possible to achieve more compact transceiver design with standard PCB technology, which leads to low cost. In this paper, the simulation of broadside coupled differential pair based design is presented. Based on the 3D simulation of this PCB by CST, we find that this broadside coupled differential structure can operate up to 20 GHz with a worst case loss of 3.42 dB. Finally, the broadside coupled differential pair based PCB for 10 Gbps transmitter is assembled as a preliminary prototype.

Introduction

The required interconnect bandwidth is increasing exponentially for the data centers (DC) and high-performance computing (HPC) infrastructures [1]. Compared to the electrical interconnects, the optical interconnects have many advantages such as small footprint, high bandwidth density and data rates [2]. Therefore, they are identified as the promising solution to support the projected increased performance of a factor of 1000 every 10 years [3]. However, current VCSEL-based transmitter assembly requires many expensive and complicated packaging processes, which limits massive penetration into the market.

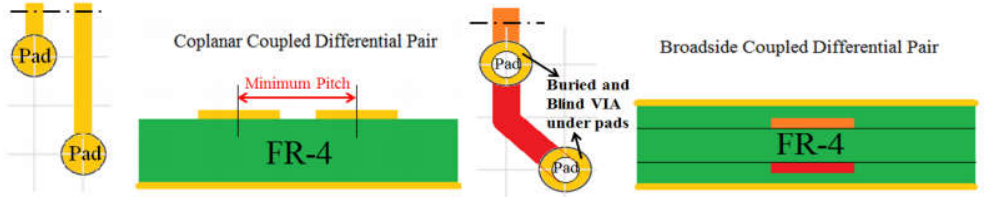
Printed Circuit Board (PCB) technology plays an essential role in the development of most modern electronic products. In particular, the FR4-based PCB, compared to interposer based transmitter modules [5, 6], is well known for its low-cost, multilayer structure and ease of fabrication process. However, its minimum pitch is limited to 150 μm due to the current PCB technology and a coplanar differential structure, which is widely used, cannot be properly incorporated into the PCB design under these constraints. As a result, the packaging of the transmitter ultimately impacts the final form factor and/or requires more expensive fabrication processes.

In this paper, we exploit the broadside coupled differential structure on standard PCB technology to match the narrow pad pitch of CMOS drivers that are used to control 850 nm VCSELs. Firstly we validate robustness against PCB fabrication process variation. Secondly based on the 3D simulation of this PCB by CST (Computer Simulation Technology), we find that this broadside coupled differential structure can operate up to 20 GHz with 3.42 dB loss. Finally we discuss assembly aspects of a prototype.

Broadside coupled differential pairs

There are two different types of differential pairs: edge coupled and broadside coupled. Compared to the edge coupled differential pair, the broadside coupled differential can offer small footprint, which will not only enhance the electronic integration but also support more compact design. As a result, this structure could reduce the size of the entire system and improve the bandwidth density.

Also, the broadside coupled structure provides a low-cost method to overcome the fabrication limitation for the small pad pitch with the standard technology. For example, the pitch width of differential pair input of the driver IC is only 125 µm. Because of such small pad pitch, the edge coupled differential pair, normally utilized in high-speed interposer design, cannot be fabricated on PCB: the minimum possible pitch is limited to 150 µm (as depicted in Fig. 1a). The broadside coupled structure then is a useful alternative for high resolution pad pitch electronics (see Fig. 1b).

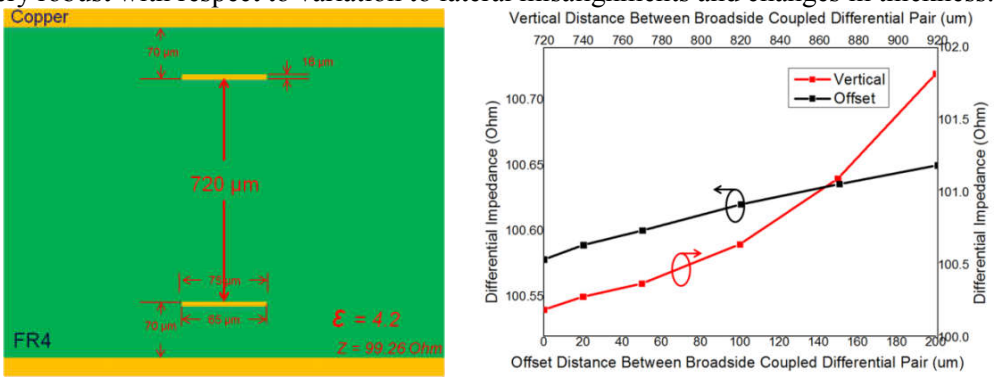


(a) (b)

Fig. 1: (a) Top-view of PCB routing with coplanar coupled structure and cross-section at dashed line; (b) Top-view of PCB routing with broadside coupled structure and cross-section at dashed line.

Impedance simulation for broadside coupled differential pair

The differential impedance of this structure is simulated by a tool for PCB, the field solver- Polar SI 9000. In order to reduce the unwanted reflections, the differential impedance should be 100 Ohm. The detailed geometry of the broadside coupled structure for this transmitter is shown in Fig. 2a. We use the simulation tool to investigate how the differential impedance varies as a function of fabrication deviations. The simulation result (See Fig. 2b) shows that this packaging approach presents a large manufacturing tolerance against misalignment (within ±100 µm in offset) in PCB multilayer bonding process and against any thermal expansion possible (within ±100 µm in thickness) after high temperature reflow. In both cases the worst case differential impedance never exceeds 101.7 Ohms. This shows how this differential pair structure is very robust with respect to variation to lateral misalignments and changes in thickness.



(a) (b)

Fig. 2: (a) Geometry (lateral view) of the broadside coupled differential pair for this optical transmitter (b) Differential impedance VS changing the offset and vertical distance between differential pairs.

3D simulation using CST

The CST software package is used to perform a full 3D simulation for the designed and fabricated 4-layer PCB, shown in Fig. 3a, in order to investigate the frequency response of the implemented broadside coupled differential pair including all real world constraints. In Fig. 3a, the inputs are two rectangle pads on the surface layer with 250 µm pitch for RF probes and the output are square pads on the bottom layer for the flip-chip bonding. The broadside coupled differential pair is in two inner layers. Also blind

and buried VIAs are used to make connections between layers. The transmission parameter S11 and reflection parameter S21 for this model are shown from 0 to 25 Ghz respectively in Fig. 3b and 3c. The blue curves are the results for an ideal structure without pads and VIAs. The results associated with the real broadside coupled differential pair including unbalanced VIAs and Pads are shown as red curves. Based on the port mode results, the differential impedance between the pads for RF probe is 86.05 Ohm, while the differential impedance for output pads is only 62.19 Ohm, which is compatible with the layout of the chip though. Due to these impedance and length mismatching, this structure suffers the extra reflection and timing problems compared to the ideal case. To improve the high speed performance, pads for the connector can be designed to fulfil 100 Ohm differential impedance.

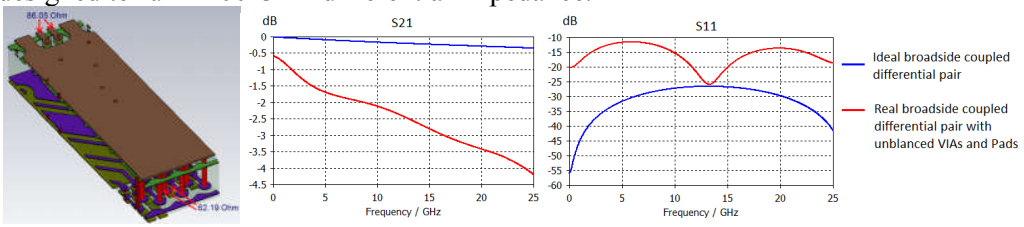


Fig. 3: CST Simulation of Transmission and reflection parameter for broadside coupled differential pair;

Based on the 3D CST simulation, the ideal broadside coupled differential pair shows excellent permanence: the transmission coefficient slightly decreases from -0.012 dB at 0 Hz to -0.035 dB at 25 GHz and the reflection coefficient is below -25 dB. Compared to the ideal structure, the implemented broadside coupled differential pair needs to use unbalanced VIAs and pads to provide the electric connection to the chip, which introduces the unwanted reflection and extra loss. The transmission coefficient (S_{21}) is -0.06 dB at 0 Hz and -4.2 dB at 25 GHz and the reflection coefficient (S_{11}) shows a fluctuating curve between -11.8 dB and -26 dB across the same frequency range. The main cause of these fluctuations is the length mismatch between the two transmission lines.

Schematic module in CST is also used to do the corresponding eye diagram simulation for real broadside coupled structure, which are shown in Fig. 4 at 10 Gbps and 20 Gbps. The eye diagram is clearly open even at 20Gbps. Due to the length difference in the real broadside coupled differential pair with unbalanced VIAs and pads, the timing problem become significant at 25 GHz. In order to solve the timing problem, the length difference need to be accurately calculated and should include not only the length mismatch of the broadside coupler traces but also the blind and buried VIAs.

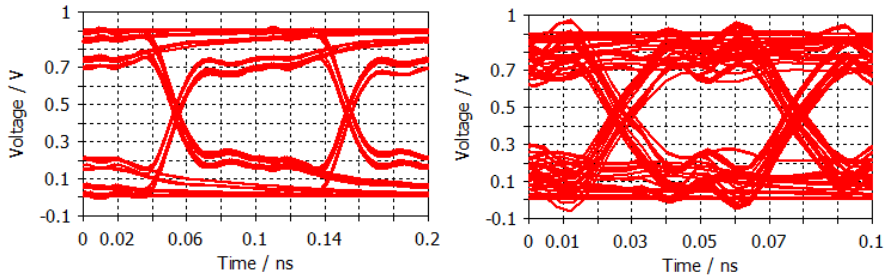


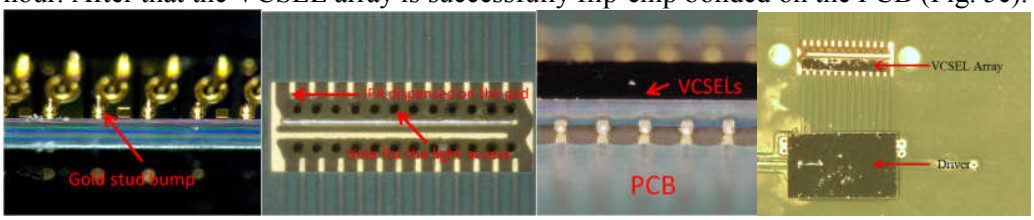
Fig. 4: CST Simulation for eye diagrams of broadside coupled differential pair at 10 Gbps and 20 Gbps;

Because the signals need to propagate from the input pads (most likely the BGA pads of the ASIC generating the high speed signals) to the place where they are transformed to the broadside coupled pair the relative position of the pads can be used to compensate

for the timing difference. In addition also changing the offset between the broadside coupled traces can be used as we have shown that small offsets have a minor effect on the eventual impedance (Fig. 2b). Using these techniques we believe broadside coupled structures can show better performance and function well at 25 GHz or even higher frequency.

PCB Assembly Processes

In order to demonstrate this low-cost method, a 4-layer broadside coupled structure based PCB for 10 Gbps optical transmitter has been fabricated. To assemble the PCB, gold stud bumps are ultrasonic formed on the pads of the VCSEL arrays (Fig. 5a) and the Isotropic Conductive Adhesive (ICA) -epoxy H20E is dispensed on the pads of PCB(Fig. 5b). Then the flip-chip bonding with the FINEPLACER® lambda Die Bonder is applied between stud bumps and ICA- epoxy H20E for 150 °C for 1 hour. After that the VCSEL array is successfully flip-chip bonded on the PCB (Fig. 5c).



(a) (b) (c) (d)

Fig. 5: (a) Stub bumps on VCSEL array; (b) Dispense the ICA epoxy H20E on PCB. (c) Flip-chip bonded VCSEL array on PCB. (d) Assembled broadside coupled differential pair based optical transmitters;

The driver IC, supplied with SnAg solder bumps, is flip-chip bonded onto the PCB using a reflow process at 237 °C for 12 seconds. The fully assembled broadside coupled transmitter is shown in Fig. 5d.

Conclusion

In this paper, we propose a low-cost structure: broadside coupled differential pair, which can achieve ultra-narrow pitch tracks on FR4 with standard PCB technology. The simulation shows this structure allows large fabrication tolerance. Based on the 3D simulation of this PCB by CST, we find that this broadside coupled differential structure can operate at 20 GHz with the loss of 3.42 dB. As a low-cost solution, this broadside coupled structure has high potential to allow high speed differential pair based transceivers with standard PCB technology. To show a preliminary concept exploitation, the broadside coupled differential pair based PCB for 10 Gbps transmitter is fabricated and assembled.

Acknowledgement

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