A 64 Gb/s PAM-4 transimpedance amplifier in 0.13 µm SiGe BiCMOS

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We present a transimpedance amplifier (TIA) for optical links, implemented in 0.13 µm SiGe BiCMOS and capable of 64 Gb/s 4-level pulse-amplitude modulation (PAM-4) reception. Paired with a 0.55 A/W photodiode, a bit-error rate (BER) of 10^{-3} is achieved for 56 Gb/s (64 Gb/s) for average optical input powers between −8.4 dBm (−7.0 dBm) and at least 1.6 dBm (1.7 dBm) by switching between a high and low gain mode, selected using an on-chip digital gain control circuit. The TIA consumes 150 mW and 134 mW in these respective modes, yielding a 2.34 pJ/b efficiency for 64 Gb/s.

Introduction

The increasing popularity of multimedia applications drives an explosive growth in bandwidth requirements in datacenters. In order to meet these requirements, the IEEE has set up a task force aiming to define a 400 Gb/s Ethernet specification. One of the solutions proposed by this task force entails 8 wavelength-multiplexed streams of 50 Gb/s 4-level pulse-amplitude modulation (PAM-4) signals over single-mode fiber [1].
PAM-4 maps two bits to a symbol with normalized signal levels $+1$, $+1/3$, $-1/3$, or -1. When compared to non-return-to-zero (NRZ), which is the traditional modulation format for these applications and maps only one bit to a symbol with normalized signal levels ± 1, PAM-4 thus allows twice the data throughput for a similar bandwidth. However, PAM-4 presents new challenges to the design of both transmitter and receiver, in particular the first stage of the receiver, i.e. the transimpedance amplifier (TIA). First of all, the use of multi-level modulation poses an increased linearity requirement on the amplifier. In order to maintain this linearity over a large range of optical input powers, some form of gain control is required. Moreover, as the minimal level spacing is now only one third of the NRZ level spacing, the sensitivity of the receiver is severely impaired. Finally, PAM-4 reception is more susceptible to the effects of intersymbol interference because, in the worst case, the interfering symbol is three times as large as the desired symbol [2].
This work will first examine the architecture of a TIA designed for PAM-4 signaling up to 64 Gb/s, where we will discuss how the aforementioned challenges regarding PAM-4 reception have been dealt with. Next, experimental PAM-4 results are presented for 56 Gb/s and 64 Gb/s along with the measurement setup used to validate the TIA. Thanks to a modified test setup, an improved assembly and the use of gain control, we were able to greatly improve the TIA performance compared to our preliminary results presented in [3].

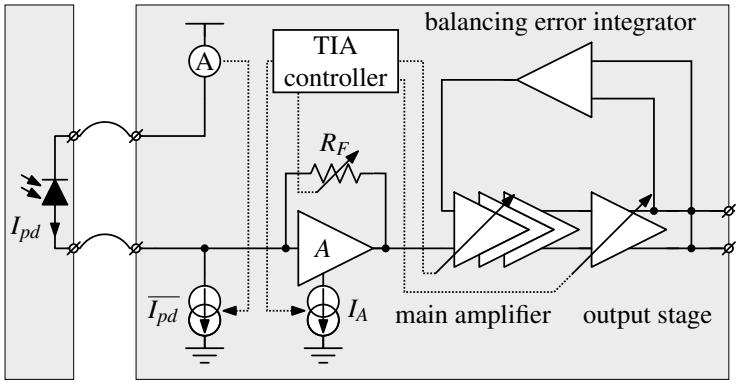


Figure 1 – TIA architecture block diagram.

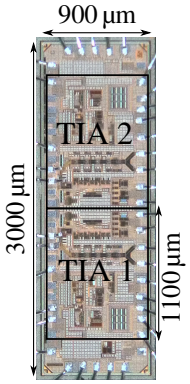


Figure 2 – Die micrograph.

TIA architecture

Figure 1 shows a simplified block diagram of the TIA [4]. The datapath consists of a single-ended shunt-feedback TIA input stage, followed by a differential main amplifier and output stage. The balancing error integrator closes a feedback loop which removes the dc-offset between both output signals by adjusting the dc-voltage at the inverting input of the main amplifier. The average photocurrent $\overline{I_{\mathrm{pd}}}$ is measured at the cathode of the photodiode and mirrored at the input of the TIA input stage, thus removing any dc-bias from the feedback resistor. This ensures the input stage is always appropriately biased, regardless of optical input power. Furthermore, the gain and associated linearity of the data path can be digitally varied using the built-in controller. The feedback resistor R_F can be modified in order to decrease the transimpedance gain for large optical input powers. In order to counteract the effect of a changing R_F on the dynamic behaviour of the TIA, the amplifier gain A is adapted together with R_F by adjusting the bias current I_A. Finally, the gain of the main amplifier and output stage can be changed as well by modifying the emitter degeneration in each stage, such that the output signal swing can be kept at a reasonable level for varying optical input powers.

The TIA runs off a 2.5 V supply and draws 134 mW to 150 mW per channel, depending on the selected input stage bias current I_A. A die, containing two identical TIAs, was manufactured in a 0.13 µm SiGe BiCMOS process and is shown in Fig. 2. Each TIA occupies 1100 µm $\times$ 900 µm. One of these TIAs was wirebonded to a PIN photodiode which was adapted for high-speed applications from [5]. The photodiode capacitance is 110 fF, while its responsivity is 0.55 A/W.

Experimental setup

The performance of the TIA was evaluated using bit-error rate (BER) and eye diagram measurements. The experimental setup for these measurements is shown in Fig. 3. The transmitter hardware is comprised of a continuous-wave 1550 nm laser, cascaded with a variable optical attenuator (VOA) in order to vary the input power at the receiver, and a 25 GHz Mach-Zehnder Modulator (MZM), modulated by an electrical PAM-4 signal yielding a 5.9 dB ratio between the optical powers corresponding to the normalized levels $+1$ and -1. This signal was generated using an arbitrary waveform generator (AWG), which in turn was fed with samples generated in Matlab.

At the receiving end, the optical signal is converted to an electrical current and subse-

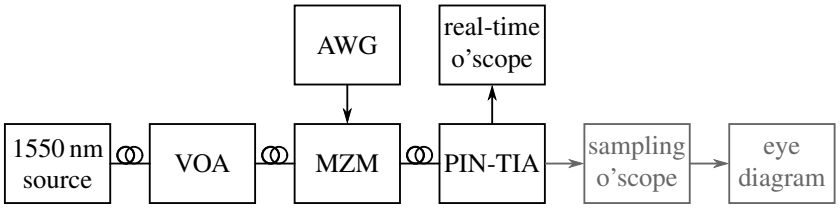


Figure 3 – Experimental measurement setup block diagram.

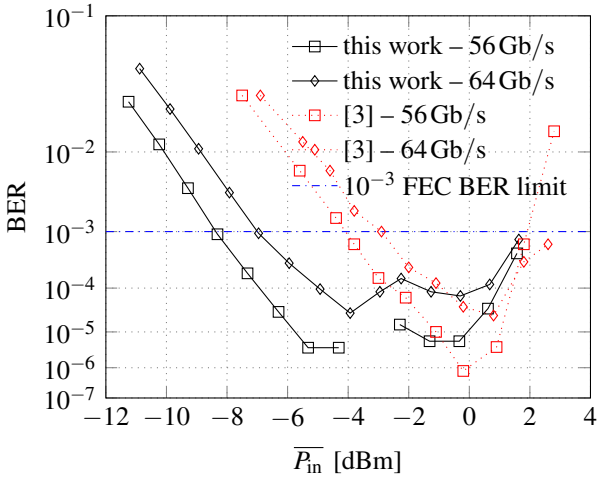
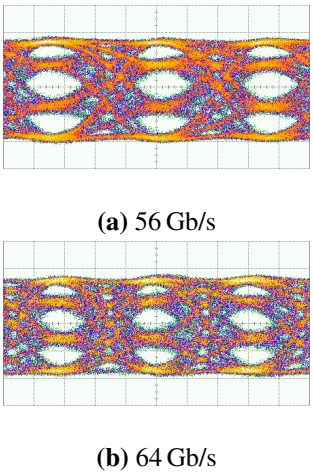


Figure 4 – Measured BER, combining the high and low gain modes, compared with our preliminary results [3], for 56 Gb/s and 64 Gb/s PAM-4.



(a) 56 Gb/s

(b) 64 Gb/s

Figure 5 – Measured differential output eye diagrams. Horizontal and vertical scale is 10 ps/div and 100 mV/div.

quently to a differential voltage by the combination of PIN photodiode and TIA (PIN-TIA). This differential voltage is then captured at 160 GSa/s using a 63 GHz real-time oscilloscope. Eye diagrams were captured using a 70 GHz sampling oscilloscope.

Results and discussion

BER measurements were performed for two TIA modes: a high gain and low gain mode, both were evaluated at 56 Gb/s and 64 Gb/s. The results of the BER measurements are shown in Fig. 4, along with our preliminary results [3] and the forward error correction (FEC) BER limit of 10^{-3}. The BER curves are the combined result of both high and low gain modes, at each point utilizing the mode yielding the lowest BER. As can be seen in the figure, the BER limit at 56 Gb/s (64 Gb/s) is achieved for average optical input powers between −8.4 dBm (−7.0 dBm) and at least 1.6 dBm (1.7 dBm) when selecting the appropriate TIA mode. Eye diagrams were measured at an average optical input power of −4.4 dBm with the TIA set to high gain and are shown in Fig. 5.

Our results are summarized and compared to publications which show BER measurements for PAM-4 at similar bit rates in Table 1. The present work shows the lowest reported power consumption; consequently our 64 Gb/s result yields the best reported energy efficiency at 2.34 pJ/b. [6] and [7] present more complex experiments for which the TIA plays only a small role; their BER results are achieved using power-hungry digital signal processing techniques such as a feed-forward equalizer (FFE) and a decision-feedback equalizer (DFE). Furthermore, one of [6]'s results is achieved using

	bit rate	**TIA power**	**input power for BER=10^{-3}**		**comments**
	Gb/s	mW	dBm (min)	dBm (max)	
[6]	52	530	-14	> -2	FFE & DFE
	52	270	-20	> -4	APD, FFE & DFE
[7]	40	N/A	-23	> -10	EDFA, FFE & DFE
[8]	50	1200	-4.4	> 4	
	56	1200	-2.4	> 4	
	60	1200	-1.3	> 4	
[3]	50	165	-5.2	2.2	
	56	165	-4	2	
	64	165	-3	> 2.5	
this	56	150	-8.4	> 1.6	
work	64	150	-7	> 1.7	

Table 1 – Comparison with the state of the art.

an avalanche photodiode (APD), whereas [7] used an Erbium-doped optical fiber amplifier (EDFA) with 25 dB gain in front of the photodiode to significantly boost the received input power. These factors have to be taken into account when comparing the TIA performance based on the BER results.

Conclusion

We have presented a TIA for optical links, implemented in 0.13 µm SiGe BiCMOS and capable of 64 Gb/s PAM-4 reception. The FEC BER limit of 10^{-3} is achieved for 56 Gb/s (64 Gb/s) for average optical input powers between −8.4 dBm (−7.0 dBm) and at least 1.6 dBm (1.7 dBm). At 2.34 pJ/b, the energy efficiency of the TIA is the best reported among publications which show BER measurements for PAM-4 at similar bit rates.

Acknowledgement

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