Embedded Opto-electronic Die Based on Wet Etched Silicon Interposer for 3D packaging with CMOS IC

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In this paper, we propose a novel way for 3D packaging of optical and electrical dies for parallel optical interconnections based on silicon interposer. With deeply wet etching of silicon, a cavity is formed for embedding and flip-chipping of optical die, and the windows for optical I/Os are opened. The CMOS IC is flipped and bonded on the top of cavity. The electrical interconnections are designed with impedance matched traces. The heat transfer is also simulated to validate the thermal isolation between dies.

Introduction

Nowadays, parallel optical interconnects are being increasingly employed in data centre (DC) and high performance computing systems (HPC), due to the advantages of optical communication and exponential growth of data traffic [1]. Electro-optical transceivers play a key role in optical interconnects, converting electrical signal to optical signal and vice versa. The combination of their cost, form factor and bandwidth dominate the decision process to use either electrical or optical communication [2]. Pluggable transceiver are presently deployed in the DC, however, with the bandwidth increasing, the size of the transceivers should reduce to fit more of them in the fixed front panel of switch [3]. In addition, to overcome the limitation of electrical connections on the switch board, optical transceivers will gradually be integrated closer to switch ASIC [3]. This requires transceivers with an ever smaller footprint.

The 850 nm multimode opto-electronics (VCSEL, PD) are favored for short reach interconnects within DC, but a cost effective packaging of opto-electronic dies and CMOS IC is required. Three dimensional (3D) packaging is an alternative to offer high bandwidth density and high performance at same time [4]. However, the thermal coupling between the stacked dies is always a big challenge for the 3D integration [5].

Silicon is a good carrier for circuit patterning, and it has been used for 2.5D packaging of opto-electronic die and CMOS IC [6]. In this paper, we embedded the opto-electronic die in a silicon interposer for 3D packaging. The novel silicon interposer, including short traces from CMOS IC to optical die and fan out traces from input/output of CMOS IC, is mainly made by wet etching and electro-plating. Besides, in order to decouple the thermal crosstalk, a layer of air between the dies will be formed after assembly, which acts as a thermal isolation layer. By using thermal simulation, we show that the air gap indeed supports the thermal decoupling of the two dies and allows the optical die to operate at a temperature which is 3.3 ℃ lower than that of the CMOS IC.

Concept of Assembly

The pads on CMOS IC are located at the perimeter of the chip area for further connection and packaging, and we propose to use the central area for opto-electronic die assembly. The package of transmitter/receiver module scheme is shown in Fig.1, where both front and backside of the silicon interposer are utilized for electrical and optical connection, respectively. The optical die is fit in the wet etched cavity, and the depth of

cavity can be controlled by etching time. Therefore, the air gap between CMOS IC and optical die is formed after embedding. The pads on CMOS chip are routed and redistributed on the surface of silicon interposer, and the 125 μm pads on the dies are fan out to a 250 μm pitch. The optical through silicon vias, for each channel, are vertically formed by double-side etching of silicon. Then, the mechanical optical interface (MOI) is fixed at the back side, and the PRIZM® LightTurn® System is utilized for light coupling into standard fiber array. The footprint of this 10 Gb/s 12-channel transmitter and receiver module will be reduced to 4 mm × 6 mm.

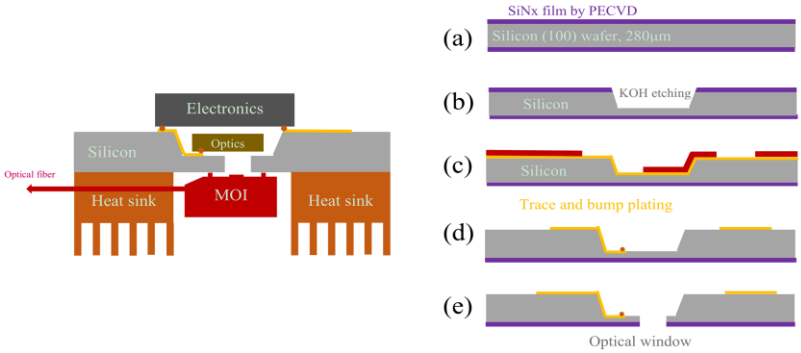

Fig.1 (left) scheme of 3D assembly of CMOS driver, VCSEL, MOI; (right) process step of silicon interposer: (a) SiNx deposition; (b) KOH etching; (c) lithography on etched topology; (d) electro-plating traces and solder bumps; (e) wet etching on both sides.

Thermal Modelling

In conventional 3D stacking, one of the biggest challenges is the thermal coupling between stacked dies. In our case, the low power optics is more sensitive to temperature. When the high power CMOS is stacked with optics, thermal isolation is essential to avoid optics being directely heated. To this end, we propose to have an air gap between them, and utilize COMSOL to simulate the heat transfer in the 3D packaged module.

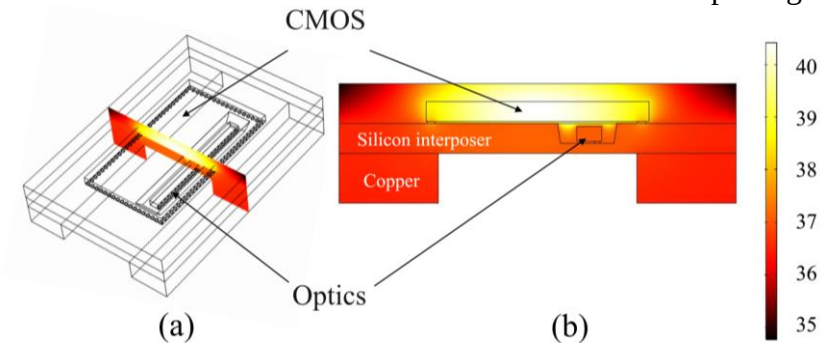

Fig.2 (a) 3D module in COMSOL, and the simulated result is selectively show in the slice area; (b) zoomed in graph of the slice plane, shows the temperature value of CMOS and optics.

The physical dimensions of the CMOS IC and optics are 3800 μm × 2250 μm × 200 μm and 3000 μm × 250 μm × 150 μm respectely. Both of them are connected with silicon interposer, 6000 μm × 4000 μm × 300 μm, through gold bumps, with the diameter of 80 μm and hight of 20 μm. The air gap between the CMOS IC and the optic die is assumed to be 50 μm after fabrication, but a scan of the air gap value is carried out to estimate the sensitivity of thermal isolation. The built module is shown in Fig. 2(a). The power dissipation of CMOS IC is assumed to be 1.02W. In the scheme, the heatsink will be connected on the backside, so two blocks of copper, 6000 μm × 1000 μm × 500 μm, are attached to the interposer. We treat the opposite side of copper as a

convective boundary, with the heat trasfer coefficient (HTC) of 5000 W/K·m^2. Front side is in air ambient, and the thickness of air is set to 400 μm. The HTC of all other boundries is set to 5W/K·m^2, nearly adiabatic. We assum the initial temperature is at room temperature (22 ℃), and the solver runs the calculation until the system is in thermal equilibrium.

The simulation result of thermal gradient for 50 μm air gap moudle is shown in Fig.2(b). The highest temperature is 40.4 ℃, on the CMOS IC, and the temperature of the optics stays at 37.1 ℃, 3.3 ℃ below the CMOS. We also investigate the thermal sensitivity to the size of the air gap with the same module in the same condition: when no air gap is present, the optics stays same temperature (difference less than 1 ℃) as CMOS IC. When thickness of air gap is major than 0 μm, the effect of thermal isolation will be more evident and eventually stable above 5 μm. Due to the air gap between the optical die and CMOS chip, the heat cannot directelly transfer to the optics. The thin layer of air is a very good isolation to avoid the thermal crosstalk. This proposed 3D scheme exhibits the thermal advatange over conventional 3D stacking approach.

Interposer Fabrication Process

The silicon interposer is fabricated on a wafer level. The patterning process includes 5 steps of lithography, and the process flow is shown in Fig.1 (right).

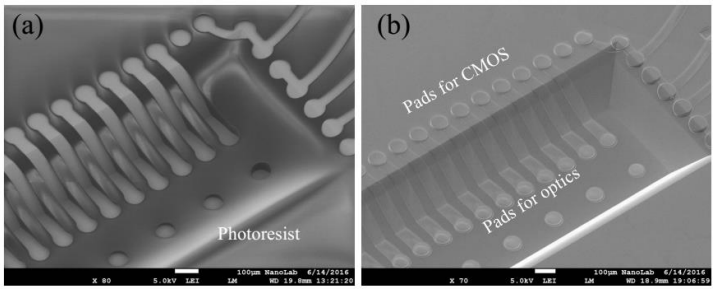

Fig. 3 (a) lithography on multilevel surface; (b) Plated gold traces and bumps.

Initially, a thin layer of SiN_x is deposited as a hard mask for wet etching, and it is selectively removed by RIE. Deeply etching of silicon is performed in KOH solution, with the etching rate of 1.0 μm/min. After 200 minutes etching, a cavity is formed with depth of 200 μm sufficient for embedding the 150 μm thick die and leave an air gap of 50 μm. Next, a uniform layer of gold is sputtered on the 3D structure. Using lithography we define (Fig. 3a) the metal traces and bumps (shown in Fig. 3b after plating). Finally, in order to get optical I/Os, SiN_x is selectively removed on both sides, and a second wet etching is performed. The processed wafer is shown in Fig. 4a. The SEM micrograph, in Fig. 4b, c, shows the vertical optical vias and the gold bumps for electrical connection.

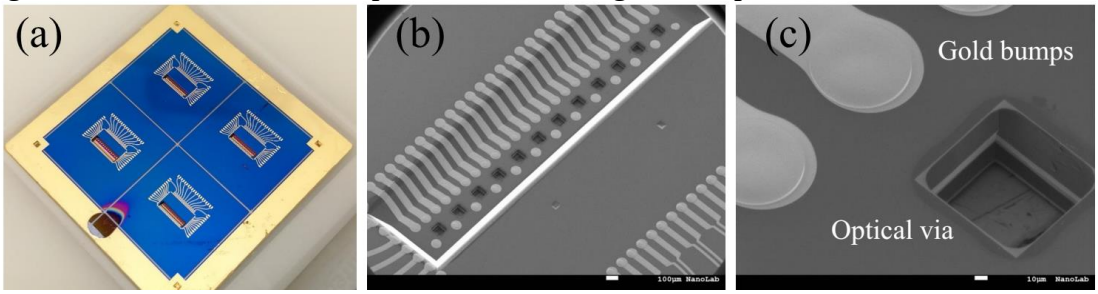

Fig. 4 (a) processed 26 mm × 26 mm wafer; (b) SEM photo of etched cavity for optics, including short traces from CMOS to optics and optical vias; (c) zoomed in SEM photo of optical via.

The flip-chip is performed on a die bonder, which is used to align and bond the dies on the completed interposer. The optical die is firstly placed inside the cavity, and the alignment of optical die is based on the pads layout and optical openings. Thermal compression bonding is used to make the gold-gold connection between the optics and silicon interposer (Fig. 5a). After that, the CMOS IC with aluminium pads is placed and ultrasonic bonded on the die bonder, in Fig. 5b. Finally, the MOI is passively aligned with etched optical vias on the other side with the same tool and fixed by epoxy.

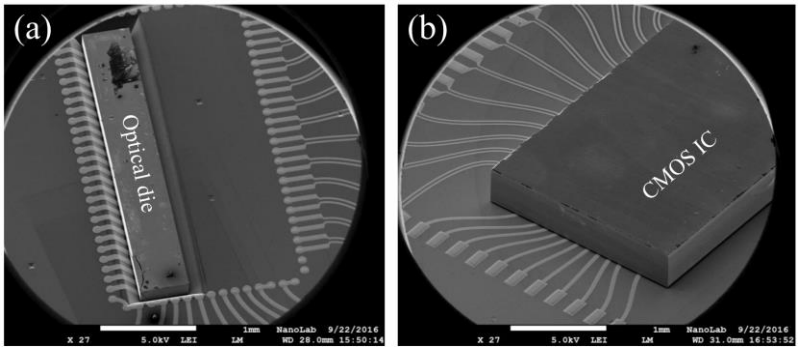

Fig. 5 (a) SEM photo of embedded optics on silicon interposer (b) SEM photo of assembled CMOS on silicon interposer and fan out traces.

Conclusion

In this paper, we demonstrated a new wafer level approach for 3D optoelectronic packaging for parallel optical interconnects. In this scheme, the impedance matched electrical connections are patterned with a single lithography step and the optical vias are obtained using a low cost wet etching process. In addition, the thermal issue of 3D stacking is solved by a designed air gap between the dies.

In the future, the performance of the transmitter/receiver module will be tested. Further, CMOS IC will be also embedded in silicon interposer by another step of wet etching. Thus, the flat surface can be obtained on the electrical connection side, and the module will be more suitable for direct mounting on other surfaces (Silicon or PCB).

Acknowledgements

This work is supported by the FP7-COSIGN project (No. 619572) and STW project-an optically connected CMOS Ethernet switch IC.

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