Standardized Layouts for Test and Assembly of Photonic Integrated Circuits

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The importance and key challenges regarding testing and assembly processes in the value chain of Photonic Integrated Circuits will be discussed. Current developments towards improved reliability, throughput via high level automation and standardization of those processes and methods from a design phase to module will be presented.

Introduction

Photonic integrated circuits (PICs) offer certain advantages over solutions based on discrete components and bulk optics, such as reduced footprint, improved stability and energy consumption [1], [2]. Increased accessibility to photonic integration technology leads to an increase of potential applications space for photonic chips. Widely present in telecommunication networks [2]–[7] the PICs also attract attention from other domains of application including data-centre networks [8], sensing [9], [10], wireless communications, millimetre and terahertz [11]–[13], cryptography [14], [15] and quantum computing [16]–[18].

A significant cost contribution to manufacturing of modules based on photonic integrated circuits can be attributed to test, assembly and packaging processes, Fig.1(a) [19], [20]. Improvements with respect to those processes can be achieved via standardization and automation which should be considered and deployed at every phase of the manufacturing chain, starting from the design phase. Here we present a standardized approach to PIC layout enabling access to automated die testing and generic assembly and packaging services, Fig.1 (b).

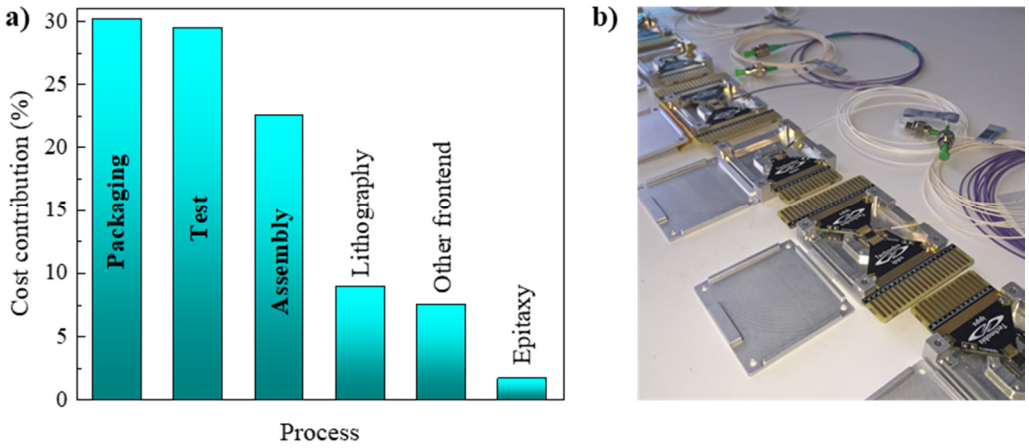

Figure 1. (a) Per-process cost breakdown (accumulated per process group) with respect to the overall cost of manufacturing of PIC based module, after study presented in [19]. (b) Generic prototyping package as offered by Technobis.

Standardized layout templates

A set of standard conventions and design rules regarding layout of PICs has been defined in line with the framework of the PIXAPP pilot line [21] as presented in Fig. 2. The scope of the definitions covers naming and allowed positions of electrical and optical IO ports, die orientation aspects, placement of fiducials supporting test and assembly processes automation and limitations imposed on the design area taking into account back-end processes and automated testing.

The die orientation should be clearly marked, e.g. with a compass rose with the directions being referenced as North, South, East and West as presented in Fig. 2. Optical ports should be placed on either East or West or on both should transmission a configuration be necessary however with a clearance from the North and South edges of a die. That clearance will depend on the type of the optical port and the particular assembly process. The electrical ports can be placed on either side of a die while placement of optical and electrical IOs on the same side is not allowed. Moreover allowed positions the electrical contacts have to respect clearance sections resulting from an overspray of coatings and/or assembly processes e.g. fiber attach, wire-bonding. Naming format of the IO ports indicates type of the port, its location on the die, and a number in a group. The label ‘dc’ or ’rf’ indicates electrical ports that can be located at north, south and west side of a chip. The ‘io’ prefix indicates optical ports that can be located either on east, west or at both sides of the PIC. The layout should also include at least three fiducials that support automation of the test and assembly process and allow to position a die in three dimensions in a unique way.

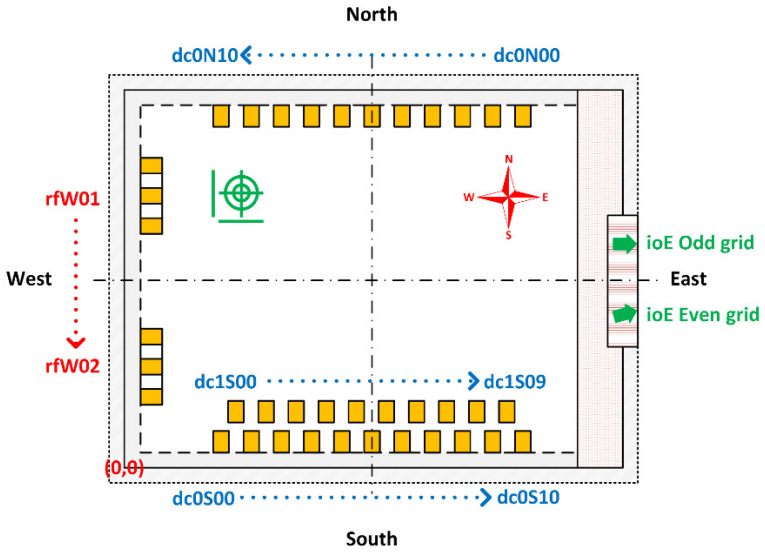

Figure 2. Standardized PIC layout setting conventions which include die orientation, input-output ports locations and naming, fiducials and assembly and packaging aspects.

In addition, size, spacing (pitch) and type of contact pads are defined within those allowed by a particular fabrication technology. An example of standard layout of electrical dc pads with all relevant dimensions indicated is shown in Fig. 3.

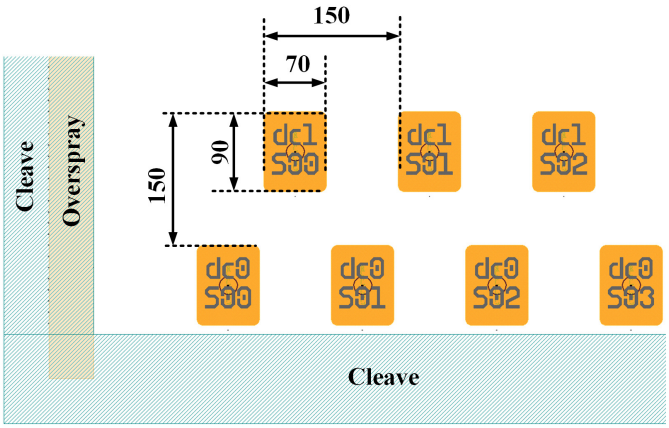

Figure 3. Example implementation of a staggered layout of electrical DC pads in Nazca design. Placement in the South of a die, two rows, pad's dimensions 70µm by 90µm and pitch of 150µm for horizontal and vertical distribution.

Implementation of those standards in electronic-photonic design automation (EPDA) tools in the form of assembly design kits (ADK) allows to take test and packaging aspects into account at an early design stage [22]–[24]. An example of implementation of such a standardized template for design of a PIC for automated die tester development and a microscope image of a fabricated chip is shown in Fig. 4 (a, b).
The EPDA tools along with a mask layout design produce a chip description file (CDF). The CDF includes description and coordinates of electrical and optical input-output ports and fiducials that can aid automation of measurement and assembly processes.

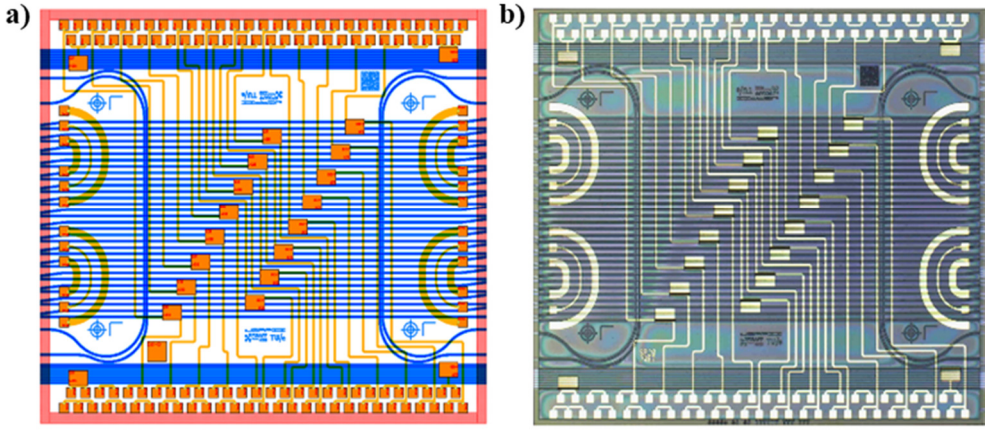

Figure 4 (a) PIC for validation of automated die tester designed according to the conventions. (b) Microscope image of InP chip fabricated in MPW run at SMART Photonics [25].

SUMMARY

The standardization of certain layout aspects reduces the extent of possible variations and enables developments of generic test, assembly and packaging services based on scalable processes with a high level of automation. In combination with availability and accessibility of foundry services for PIC fabrication through MPW runs, this opens a path for a seamless cycle from a design to module for prototyping and low to mid volume production.

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