Efficient Edge Couplers for Hybrid Integrated InP SOAs with SiPh AWGs for Low Loss WSS

Xin Ouyang, Yu Wang, Netsanet Tessema, Ripalta Stabile, and Nicola Calabretta

Eindhoven University of Technology, Dept. of Electrical Engineering, Electro-Optical Communication, 5612 AZ, Eindhoven University of Technology, The Netherlands

Abstract

The wavelength selective switch (WSS) based on photonic integrated circuit (PIC) technology plays instrumental role in dynamic reconfigurable networks. They enable to independently switch any wavelength to any output port with the compact footprint, high stability and low cost due to mass production. Hybrid integrated WSS combined with semiconductor optical amplifiers (SOAs) on InP and arrayed waveguide gratings (AWGs) on Silicon is the promising solution to provide high port count, low insertion loss, ultra-fast switching and high extinction ratios. However, due to different dimensions between InP and Silicon waveguides, high waveguide-to-waveguide coupling low loss is a challenge for hybrid integrated WSS. In this paper, we report simulated results of the efficient edge coupling solution for hybrid integration of passive Silicon AWGs and active InP SOAs. We design a laterally tapered waveguide based on III-V materials and the dual-core spot-size converter (SSC) based on SiPh to reduce the coupling loss between InP waveguide and Silicon waveguide. The proposed couplers provide higher coupling efficiency and significantly relax alignment tolerance for hybrid InP SOA gates and SiPh AWGs in-plane coupling. Comparing the simulated results, when there is no airgap between SOAs and AWGs, the alignment tolerance is doubled, and the initial coupling power is improved around 20%.

Keywords: hybrid integration; photonic integrated circuit; chip-to-chip coupling.

Introduction

With the development of 5G technology, the requirement for data processing capabilities of network facilities is constantly increasing. In order to realize dynamic and efficient processing of large heterogeneous data traffic in the next generation of metro networks, the wavelength selective switch (WSS) is designed to realize these dynamic connections. As shown in Fig.1, the hybrid WSS implemented Silicon AWGs enable large-channel passive deMux/Mux, while InP SOAs are used for fast switching and high extinction ratios. The SOAs also provide boosting to compensate the excess loss within the hybrid WSS [1]. In this hybrid-integrated WSS, a wavelength-blocker (WBL) based on Silicon AWGs and InP SOA gates is presented. However, the performance of WBL is deteriorated from high coupling loss between Silicon AWG and InP waveguides [2].

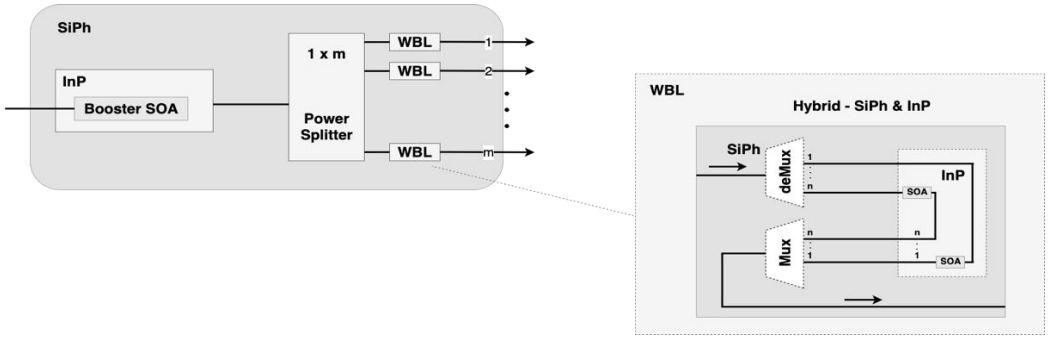

Fig. 1: Architecture of hybrid integrated wavelength selective switch.

The coupling loss can be roughly divided into two main categories: the misalignment and the mode field mismatch caused between two different waveguides [3]- [4].

For these two types of loss, we presented InP based laterally tapered waveguide and the SiPh dual-core spot-size converter (SSC) to reduce the coupling loss between InP waveguide and Silicon waveguide. The proposed couplers provide higher coupling efficiency and significantly relax alignment tolerance for hybrid in-plane coupling. Simulations are conducted under zero spacing distance between two waveguides. The coupling efficiency is simulated by varying the lateral and vertical central alignment position between the two waveguides in three scenarios: direct coupling, using Taper and using SSC. Comparing these three scenarios simulated results, the alignment tolerance is doubled, and the initial coupling power is improved around 20%.

Taper and SSC structures

A tapered waveguide was proposed for efficient coupling between deep-etched InP waveguide and 3-µm Silicon waveguide. The size of the deep-etched active layer is 1.5 µm × 0.5 µm, and the Silicon strip waveguide core is the 3 µm × 3 µm. The tapered waveguide consists of three parts: a conventional waveguide, a laterally tapered region with width tapers from 1.5 µm to 0.5 µm, and an interface region (see Fig. 2 (a)).

For the tapered waveguide structure, the tapered length was first scanned in the range 0-100 µm using the Lumerical MODE EME solver. According to the results, when the tapered length was greater than 50 µm, the transmission rate tended to stabilize, so this length was chosen as the tapered length. In addition, simulations were also carried out for different shapes of tapered waveguides, such as convex, concave and linear. From the simulation results, the tapered shape does not significantly affect the transmission efficiency of the 50 µm long waveguide. Considering fabrication, a linear waveguide was chosen for the next simulation step.

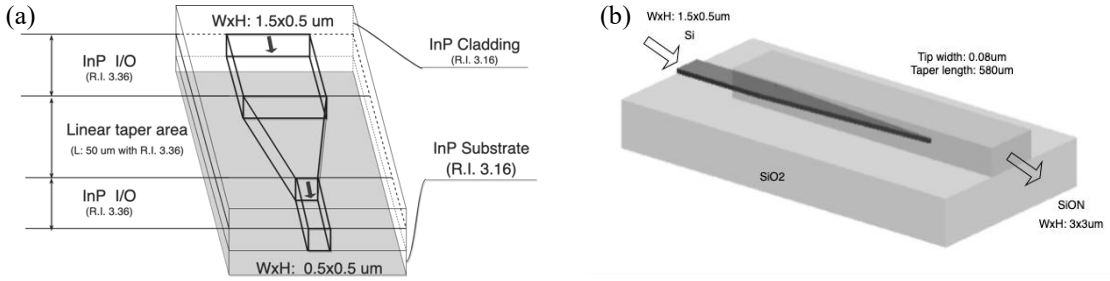

Fig. 2: Schematics of InP tapered waveguide (a) and SiPh dual-core spot-size converter (b).

To extend the mode field of the waveguide in the vertical direction, a dual-core spot size converter (SSC) is proposed, which can be divided into three parts: Silicon input waveguide, Silicon tapered zone and SiON output waveguide (see Fig. 2 (b)). At the input side, the light wave is mainly confined in the lower waveguide, which has the same dimension as the tapered waveguide input. Then inside the taper zone, as the waveguide width gradually decreases, the waveguide mode gradually tends to cut off, and the electromagnetic field penetrates the upper waveguide. The dimension of the upper waveguide is 3 µm x 3 µm with SiON. With this dual-core SSC, the output mode field can also be expanded vertically and match the Silicon waveguide.

Same as tapered waveguide, the proposed structure is first to be optimized in Lumerical MODE EME solver. The length of the lower tapered waveguide is sweep in the range of 0-1000 µm. Moreover, between 0 and 1.2 µm, 7 points are chosen for optimizing the tip width. After optimizing, 500 µm long lower tapered waveguide and 0.08 µm tip width is chosen for further simulation.

For the Silicon and InP waveguide facets, they have been coated by AR-coating to reduce reflection loss. A 198 nm thick single-layer SiN (refractive index 1.95) coating is used for Silicon, and a single layer with a refractive index of 1.83 and 211 nm thick is used as the coating of InP.

Simulation Results

For structure optimization, the Lumerical MODE EME solver is used. For conducting coupling simulations, both optimized structures are implemented in Lumerical FDTD. Then after propagating through the entire Tapered waveguide and SSC and 1 µm airgap, one monitor is placed after 1 µm inside Si-based waveguide. Using mode profile which Si-monitor received, overlap with fundamental TE/TM mode profile of Si-waveguide to get the mode power coupling. All simulations are carried out with the center wavelength of the C-band at 1.55 µm.

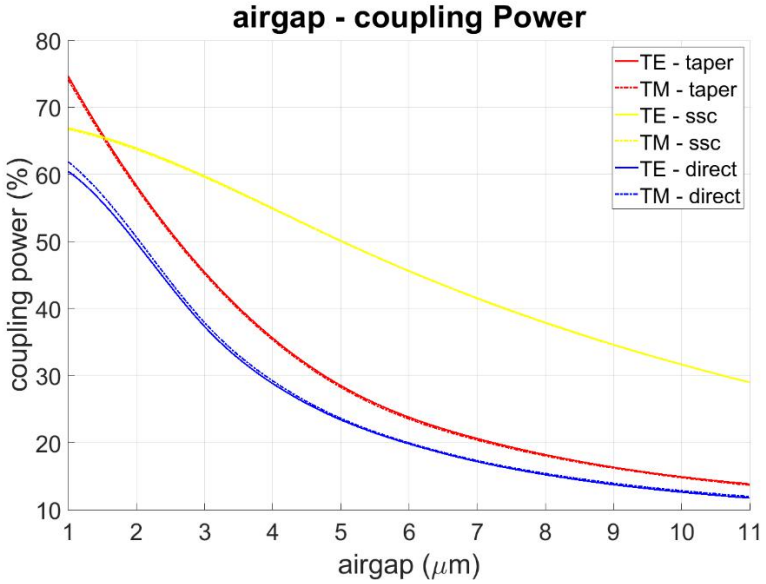

Fig. 3: TE/TM mode power coupling after different airgap between waveguides

After implementing a tapered waveguide or spot-size converter, the initial energy has been increased by 25% and 13% respectively. In the axial direction, spot-size converter can provide a much larger coupling pitch compared to tapered waveguides. For the tapered waveguide, the tolerance is relaxed from 2 µm to 2.6 µm to keep 50% mode power compared to direct coupling. With SSC, the tolerance in the axial direction is improved to 5 µm, which is 1.5 times compared to directly coupling.

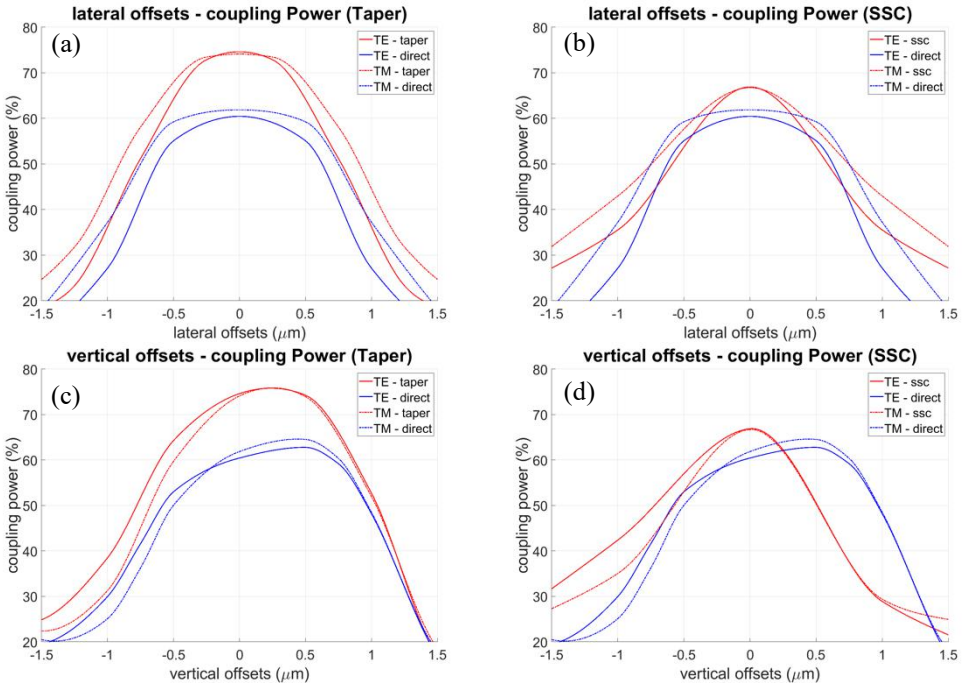

Fig. 4: TE/TM mode power coupling under different lateral (a)(c) and vertical offsets(b)(d)

At 1 μm airgap distance between two waveguides, directly coupling needs to keep 1.2 μm in lateral and 1.5 μm in the vertical direction to keep 50% mode power. With a tapered waveguide, tolerance is relaxed to 1.6 μm in the lateral direction and 1.85 μm in the vertical direction.

Conclusions

The simulation results show that the coupling efficiency can be effectively improved by placing tapered waveguides or SSCs. With a 1 μm airgap, the initial energy has been increased by 25% for tapers and 13% for SSC respectively. Meanwhile, the alignment tolerance is also effectively improved. The dual-core SSC could provide a significant 1.5 times relaxed tolerance in the axial direction, and the tapered waveguide can provide a 25% average improvement while aligning in the lateral and vertical direction.

Acknowledgments

This project has received the funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska-Curie grant agreement 814276.

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