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Trans-impedance two stages OEIC Receiver using PIN Photodetector

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This paper deals with the design of a broadband low-noise receiver for fiber optical transmission systems. A high-impedance first stage is designed in order to minimize all sources of noise. Then, a second stage performs the required equalization in order to restore the signal shape, which is distorted owing to the limited bandwidth. The proposed optoelectronic receiver is theoretically analyzed. A simplified noise model is also developed. Computer simulations, performed vith MDS, are carried out, based on a complete electrical model library. The latter includes wideband noise models for normally-off and normally-on p-HEMT's [1]. The designed low-noise amplifier exhibits a 40 dB constant trans-impedance gain over a 44 MHz-40 GHz frequency range.

Introduction

One fundamental design criterion for optical receivers is to minimize the amount of the optical input power needed to achieve a given bit error rate or a given signal to noise ratio in analog systems. Consequently the front-end receiver, which amplifies the electrical signal provided by the photodetector, has to be accurately designed, as the amount of noise present in the pre-amplifier is directly related to the receiver sensitivity. The simplest receiver front-end consists of a photodetector, an input resistor and a low input impedance amplifier. As the thermal noise associated with the input resistor is one of the principal elements which determines the amplifier noise performance, it will be possible to minimize the receiver noise by maximizing the amount of voltage on the input resistor. This approach allows to remove low value shunt resistors and high value series resistors which dramatically reduce the noise performance. Unfortunately the input resistor, used to convert the photocurrent in a signal voltage, reduces the bandwidth of the system via the RC time constant, where the capacitance is the total input capacitance of the first stage. The influence of the input resistor and input capacitance will be compensated by an equalizing stage.

Design and optimization

This section describes the proposed receiver configuration and shows how to determine both signal to noise ratio (SNR) and circuit bandwidth.

A. Noise analysis

In this section we analyze the amplifier noise performances. Our analysis takes into account only the high-impedance front-end, because, as in a cascaded network, the noise factor is primarily influenced by the first stage noise. Theoretically, the noise of the receiver can be minimized by presenting an optimum source impedance to the amplifier. As the source impedance and noise generators of the photodetector are function of the frequency, in a practical design, matching networks which approximate

the required optimum impedance, can be obtained only with high order lossless filters, which are not realizable over a wide frequency range. In order to analyze the amplifier noise performances we derive the equivalent input noise current. Our approach is to calculate the total noise at the amplifier output and then to divide the output noise by the trans-impedance gain. The total equivalent input current noise can be written as:

$$i_{neq}^2(f) = \frac{v_{nout}^2}{\left|Z_{fs}(f)\right|^2} = i_{nd}^2 + i_n^2(1+C_d R_s s)^2 + V_n^2\left(\frac{(1+C_d(R_d+R_{in})s)^2}{R_{in}^2} + (1+C_d R_d s)^2 Y_c^2\right) + \frac{4K(1+C_d R_d s(2+C_d(R_d+R_{in})s))T}{R_{in}} \quad (1)$$

where K is the Boltzmann's constant, T the temperature in kelvins, and i_{nd} the photodetector current noise generator. First stage amplifier noise is represented by a zero impedance voltage generator V_n and an infinite impedance current generator i_n. Y_c is a complex number derived by correlating the i_n and V_n generators. Several considerations can be made from the equation (1). It is clear that the noise for each resistor increases i_{neq}. The resistor R_{in} must be as large as possible to reduce its effect on i_{neq}. Unfortunately a large input resistor reduces the first stage bandwidth dramatically. The SNR can be simply obtained by substituting the equation (1) in the following expression:

$$SNR = \frac{i_S^2}{\int_0^{+\infty} i_{neq}^2(f)\,df} \quad (2)$$

Details for the method used to calculate the equivalent input noise current can be found in [2].

B. Bandwidth analysis

In order to design a wideband amplifier for OEIC receivers we start by analyzing the amplifier block in Fig. 1. The schematic circuit diagram shows a transistor where an admittance Y_F forms a parallel feedback and Y_E forms a series feedback path. The

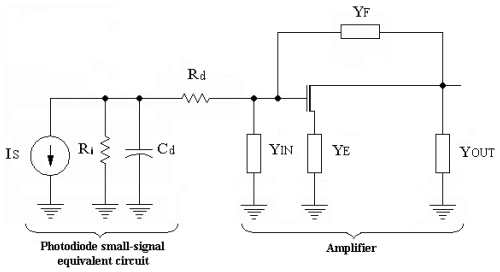


Fig 1. Small signal equivalent model for the PIN photodiode and a generic stage of the amplifier

circuit analysis was performed by using the nodal approach. The main block, represented by the transistor and the two feedbacks, can be described in terms of nodal

admittance matrix. As the Y_E admittance is grounded, we can define a 2x2 admittance matrix:

$$Y = \begin{pmatrix} y_{11} - \dfrac{(y_{11}+y_{12})(y_{11}+y_{21})}{y_{11}+y_{12}+y_{21}+y_{22}+Y_E} + Y_F & y_{12} - \dfrac{(y_{11}+y_{12})(y_{12}+y_{22})}{y_{11}+y_{12}+y_{21}+y_{22}+Y_E} - Y_F \\ y_{21} - \dfrac{(y_{11}+y_{21})(y_{21}+y_{22})}{y_{11}+y_{12}+y_{21}+y_{22}+Y_E} - Y_F & y_{22} - \dfrac{(y_{12}+y_{22})(y_{21}+y_{22})}{y_{11}+y_{12}+y_{21}+y_{22}+Y_E} + Y_F \end{pmatrix} \tag{3}$$

Where y_{11}, y_{12} , y_{21}, and y_{22} represent the Y-parameters of the active device. For low noise design purpose a high impedance first stage has been proposed. This configuration is obtained by imposing $Y_F = 0$, Y_E infinity, and Y_{in}, Y_{out}, determined by considering the input and output load. The trans-impedance Z_{fs} of the first stage can be written as:

$$Z_{fs} = \frac{V_{out-fs}}{i_s} = \frac{g_m R_{in}}{g_{ds}[(1 + s C_{gs} R_{in}) + s C_d (R_{in} + R_d (1 + s C_{gs} R_{in}))]} \tag{4}$$

where the photodiode junction resistor R_i has been neglected and C_{gs}, g_{ds}, g_m, are the elements of the small-signal equivalent circuit for the transistor. The transistor model has been simplified in order to present a simple analytic solution. The transfer function in (4) exhibits two poles, but only one, located at low frequency, determines the high-impedance behavior of the first stage. In order to obtain a flat response up to high frequencies, we cascode the first stage with an equalizing stage characterized by a zero located such as it cancels the integrator pole. We consider a second stage where the parallel feedback is a resistance R_f, whereas the series feedback is composed of a resistance R_{eq} and a capacitance C_{eq} connected in parallel. The second stage voltage to voltage transfer function is:

$$H_{ss} = \frac{V_{our-ss}}{V_{out-fs}} = A_V \frac{s - z}{z - p} \tag{5}$$

with:

$$p = -\frac{R_L + (g_{ds} + g_m) R_{eq} R_L + R_f (1 + g_m R_{eq} + g_{ds} (R_{eq} + R_L))}{(C_{eq} + C_{gs}) R_{eq} (R_f + R_L + g_{ds} R_f R_L)}$$

$$z = \frac{g_m R_f - (g_{ds} + g_m) R_{eq} - 1}{R_{eq}(C_{eq} + C_{gs} + C_{gs} g_{ds} R_f - C_{eq} g_m R_f)}$$

$$A_V = \frac{(C_{eq} + C_{gs} + C_{gs} g_{ds} R_f - C_{eq} g_m R_f) R_L}{(C_{eq} + C_{gs})\ (R_f + R_L + g_{ds} R_f R_L)}$$

where we assume two identical transistors for the first and the second stage. In order to have a zero-pole compensation we cancel the low frequency pole of the first stage with the zero of the second stage. This condition is satisfied when:

$$C_{eq} = \frac{2C_{gs} R_{eq}(1+g_{ds} R_f)+(1+(g_{ds}+g_m)R_{eq}-g_m R_f)(\sqrt{\Delta}-C_{gs}R_{in}-C_d(R_d+R_{in}))}{2R_{eq}(g_m R_f-1)} \quad (6)$$

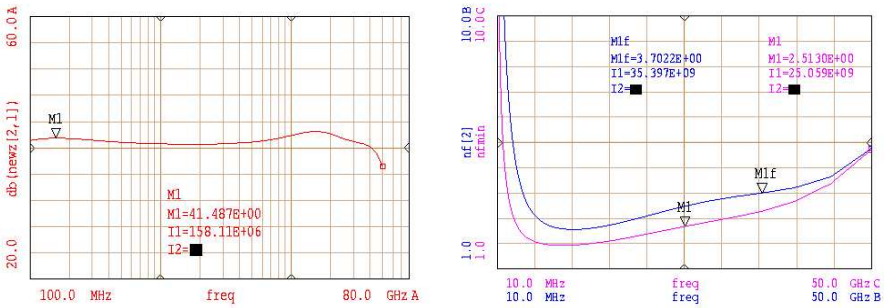
with:

$$\Delta = (C_{gs} R_{in} + C_d(R_d + R_{in}))^2 - 4C_d C_{gs} R_d R_{in}$$

Only the positive value of C_{eq} are allowed. Such values can be determined by performing an implicit plot of the equation $C_{eq} = 0$, versus positive values of R_{eq} and R_f, then by identifying the positive and negative regions.

Results and Discussions

A broadband trans-impedance amplifier has been designed on the theoretical basis presented in the previous sections. Fig. 2a shows the gain obtained with MDS circuit simulator. The 3*dB* bandwidth is larger than 40 *GHz*, while the trans-impedance gain is about 41 *dB*. Simulations have been performed by assuming a 50 Ω output port. Fig. 2b shows the amplifier noise performance in terms of noise figure. A good noise performance is assured with a high-impedance front-end. Although this approach entails a limited dynamic range, it is normally used in many high sensitivity applications [3, 4].



a) b)

Fig2. a) Trans-impedance gain, b) Noise figure and minimum noise figure.

Acknowledgments

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