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A System Demonstrator using 2-D fibre-based optical interconnect between CMOS IC's

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Abstract:

Vastly increasing interconnection problems make research groups world-wide look for solutions using optical interconnection. In the European Community funded ESPRIT project OIIC ("Optically Interconnected Integrated Circuits") an area optical interconnect approach as solution to the interconnect bottleneck encountered in advanced VLSI-CMOS designs is pursued.
The design and fabrication of a demonstrator consisting of a three chip digital system will be discussed. This demonstrator implements 256 optical I/O channels per chip (2x 8x8 out, VCSEL or RCLED; 2x 8x8 in, InGaAs photodetector arrays). Each chip, a custom CMOS design, implements digital and analogue functionality, and has the optoelectronic arrays hybridly flip-chip mounted on top. The optical links consist of arrays of plastic optical fibre.

Introduction

It is our goal to demonstrate the viability of massively parallel optical interconnects between electronic VLSI chips. This is done through the development of the technology necessary for the realization of such interconnections, and the definition of a systems architecture in which these interconnections play a meaningful role. In this paper, we present the realization of a small-scale optoelectronic FPGA with 8 × 8 logic cells, containing two optical sources and two receivers per FPGA cell yielding a total of 256 links per chip. These FPGA chips will be used in a three-chip demonstrator system as a test bed for the concepts above.
The optical components consist of two 8x8 source arrays (either LEDs or VCSELs) and two 8 × 8 InP detector arrays, which are flip-chip bonded to the CMOS circuit and actually overlay part of the CMOS circuits. Electronic driving and receiving circuits are realised in CMOS, and are intermixed with the digital circuits.
Each of the 256 optical channels is designed to operate at an information rate of 80 Mbit/s, a typical data rate for high-end commercial FPGA's. To ensure reliable communication over so many parallel channels in a noisy digital environment, AC-coupled communication with Manchester coded data is used in the design.
The optical pathways between the central chip and its two neighbours consists of removable 8 × 16 Plastic Optical Fibre (POF) ribbons. The two outer chips are equipped with 2 × (8 × 8) ribbons with horizontal insertion POF-ribbon connectors allowing a closed, toroidal interconnect, or an open optical I/O access to the system.

The System Demonstrator

On the chip, digital and analogue functionality (separate drivers and receivers for each individual optoelectronic component, and the FPGA functionality) are intermixed. For the CMOS, an external foundry service delivering 0.6µm technology is used. Aggregate bit rate (I/O per chip) will exceed 10 Gb/s.

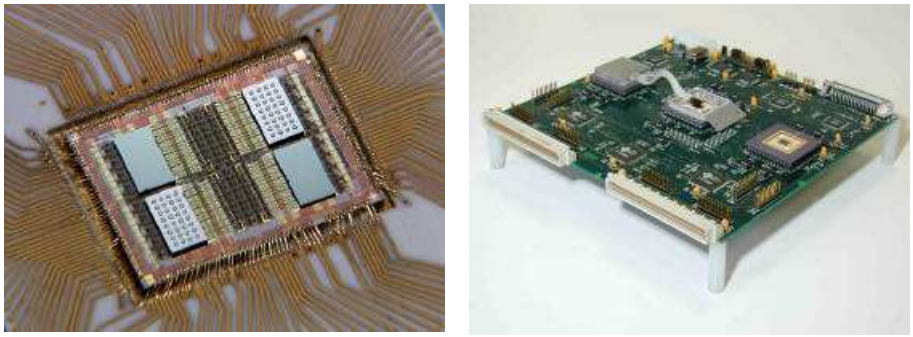

Figure 1a,b: The system demonstrator consists of 3 PGA packages, each holding a CMOS FPGA-chip with analogue drivers and receivers. On top of the CMOS, arrays of optoelectronic components are hybridised. The chips are optically interconnected by arrays of plastic optical fibre, in ribbons of 128 channels. On the right picture, 2 of the opto-assemblies are optically connected.

More on the concepts and choices made earlier on in the project can be found in [i].
The optoelectronic FPGA demonstrator is at the time of writing, in the stage of full scale testing. The coupling and passive alignment concepts have proven to be functional, repetitive connecting and disconnecting does not harm the optical pathways.

The CMOS circuit functionality

The CMOS FPGA chips are small, custom made 8 x 8 FPGA's, with an optically augmented interconnect fabric. Per configurable logic block, there are two bi-directional links, interconnecting to the corresponding points in the neighbouring electrical layers. Driver and receiver circuits were designed to be used in the 2D array configuration. Transmitter and receiver analogue electronic circuits have been geometrically adapted for placement into the 250 µm optical interconnect raster and for integration with the digital FPGA circuits. Driver and receiver cells are designed with as boundary conditions the required 160Mbit/s performance, minimal power consumption, opto-component specifications and available chip area. Measurements show, that the electronic driver and receivercircuits work according to design specifications, although the harsh environment is a critical issue, especially for the receivers.

Optoelectronic components

Efforts for transmitters are concentrated on both RCLED's and VCSEL's. Because both components offer rather different categories of advantages, it is still unclear, which of the two device types are to be preferred in this particular application area.
Although highly efficient microcavity LED's can be fabricated (external efficiencies up to 22.8 % reported [ii]), the requirement for efficient coupling to a limited (although relatively high) numerical aperture medium implies a reduction of the device efficiency.

Therefore, devices have been optimised for efficient coupling to plastic optical fibre, rather than for shear extraction efficiency[iii]. Device layout and cross section are similar to the case of the VCSEL's to ensure mounting compatibility. Details on the electrical and optical properties of these devices can be found elsewhere[iv]
In view of the rather broad radiation pattern and the diameter of the POF, rather large photo detectors are required. The diameter of the devices, 150µm, is obtained by optimising a combined efficiency - cross talk criterion, and results in a depletion capacitance of 1.4 pF

Optical Pathway

One has to realise that the choice of an optical pathway has a profound impact on the way a system is assembled at the board (or MCM) level. The best choice will not only be a function of optical performance but also of reliability, robustness, and obviously cost. The FPGA-based system demonstrator is built on a POF based approach.
Relative ease of termination together with extreme flexibility of the pathway is considered highly favourable in this context, but on the other hand, long-term reliability of the material could presumably pose problems in very demanding applications. Optical pathways have been fabricated using Toray's PGR-FB125 fibre. The numerical aperture of this fibre is high (typically 0.5), facilitating strong bending without excessive loss, and the diameter can be as small as 125µm (120 µm core). Main drawback of this medium is the rather high absorption (about 12 dB/m @ 980 nm, about 6 dB/m @ 850 nm). For bend radii larger than 2 mm excess losses do not exceed 0.5 dB/90°.

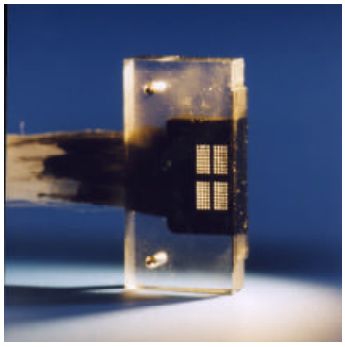

Fig 2. Endface of an optical pathway block made for the system demonstrator.

Pathways have been fabricated with 128 channels, using PMMA hole plates, with precision drilled holes for the fibres and alignment pins.

Link Experiments

Initial tests on populated system demonstrator chip show near 100% yield on transmitter and detector array flip-chip mounting, and correct CMOS functionality. Some fabrication errors are evident however on some of the chips. The supply voltage of the chip is 3.3V, and 2.5mA modulation current for an LED yields a functional link through a 20 cm long POF fibre.

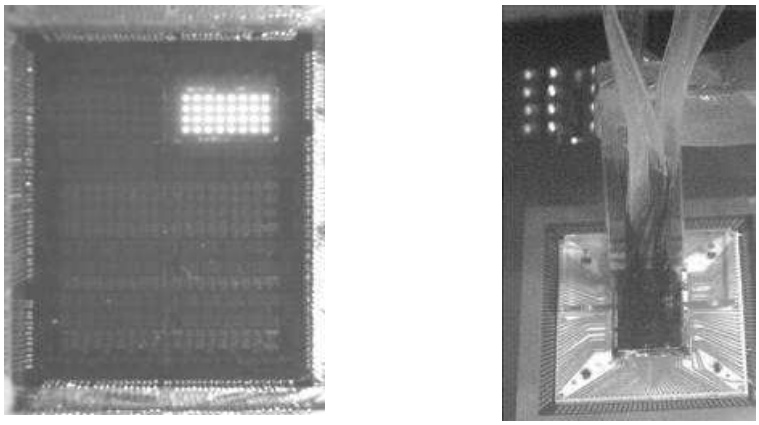

Fig 3a, b: System demonstrator chip (partially populated) with 100% working array of RCLED's. On the right: POF bridge for intra-chip measurements

A number of these first results have been reported in Brunfaut[v]. Tests have been carried out with the modules mounted on a specially designed PCB board, which enables us to compare transmission of signals by optical means in comparison to the conventional electronic way.

Conclusions

This system demonstrator enables the exploration of optical interconnect within a meaningful context. The functionality, although FPGA's are extremely versatile components, only enables us to scratch the surface of the immense parameter space, but nevertheless a lot of knowledge will be gained.

Acknowledgements

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