Direct optical injection of precise clock edges into standard CMOS circuits with short optical pulses.

Christof Debaes[1], Aparna Bhatnagar[2], Diwakar Agarwal[2],
Hugo Thienpont[1] and David A. B. Miller[2]
1 Departement of Applied Physics and Photonics, Vrije Universiteit Brussel,
Pleinlaan 2, 1050 Etterbeek, Belgium
2 Departments of Applied Physics and Electrical Engineering, Ginzton Laboratory,
Stanford University, Stanford, CA 94305-4090 USA

We report the direct injection of precise clock signals into standard CMOS circuits using short optical pulses by a novel receiver-less scheme that eliminates the delay, skew and jitter of a typical receiver. By connecting the detector to a high-impedance capacitive node, we aim at directly introducing a large voltage swing on chip, sufficient to trigger specialty high-speed circuits. We measure the response of the detectors by the technique of on-chip sampling and show a reduction in jitter compared to a TIA-receiver. After demonstrating the potential of the approach for the injection to a single point we model the usability for larger clock distribution networks.

Introduction.

Periodic clock signals play a central role in the design of present-day synchronous systems. Data in these systems must be kept synchronized despite unequal logic path delays. Maintaining synchronicity can be straightforwardly achieved by using clocks since they are providing clear timing boundaries. Transistor scaling can increase the computational bandwidth by shrinking clock cycle times. However, the associated rise time of the clock and the allowable variation in the arrival time will need to shrink proportionally, making the reliable distribution of the clock of growing importance. Clock signals are particularly affected by technology scaling as global wires become more highly resistive with the decrease of line-dimension. This increases the delay and the associated variation on the clock compared to the clock period.
Clock distribution in current microprocessors involves delivering a sharp noise-free clock to over a hundred thousand static and dynamic latches, which combined, present a capacitive load of several nanofarads. While circuit solutions are able to overcome the shortcomings of wires in the near term, more radical approaches for clocking maybe needed for future chips. Distributed PLL networks across the chip, on-chip wire-less clock distribution, salphasic clocks and optical clocks are among the most promising approaches.

Receiver-less optical clock injection

In optics it is relatively straightforward to generate high repetition rate short pulse streams using mode-locked lasers. The repetition rate of the pulse train from a mode-locked laser is solely determined by the round-trip time in the laser. Hence, fundamentally, a mode-locked laser producing sub pico-second pulses with gigahertz repetition rates can have jitter on the order of a few hundred femtoseconds or less [1,2]. Modelocked lasers have the additional advantage that the peak optical power of the pulses can be in the kilowatt range.
In this paper we will introduce the concept of direct optical injection by allowing the generated photons to directly create suitable voltage swings onto hybridized detectors

capable of triggering small blocks of digital circuits. This can be achieved by connecting the detectors to a node with only a high-impedance capacitive load and by allowing a sufficient amount of optical power on the device.
In this scheme we do not require any receiver circuit at all, and therefore are eliminating the delay, skew and jitter a normal receiver would introduce. We are thus directly trading the receiver power consumption and latency with optical power. To create a 50% duty cycle clock from the pulse train we implement a totem-pole of two detectors as shown in figure 1.

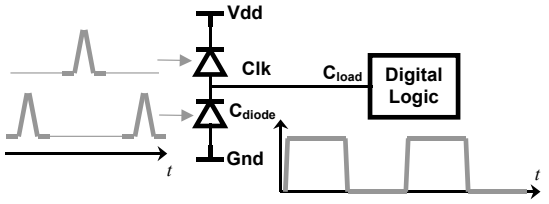

Figure 1: Schematic view of the receiver-less direct clock injection.

By alternating pulses on both detectors we are able to inject a precise square wave clock onto the chip. The approach requires a reasonable amount of optical power, but gives a number of inherent advantages in exchange. No amplifier is required and thus we are eliminating the *jitter, electrical power* and *delay* a receiver would normally introduce. One can straightforwardly shift the delay of the impinging pulse stream with a femtosecond accuracy using the combination of a translation stage and a corner-cube in the optical path. Hence, it is possible to make accurate multiphasic clocks for high-speed multiplexing or demultiplexing circuits. The signal we inject in the chip has a very high slew-rate, which will be larger than anything what can be created by the transistors on chip. The creation of these sharp edges can be exploited to trigger very specific circuits on-chip, such as samplers. This can allow more accurate on-chip timing and jitter measurements for debugging purposes. Finally, since large swings are directly created on-chip, the effect of noise on the supply rail is reduced.

Experimental Verification of the receiver-less clock injection:

We used on-chip samplers to measure the directly injected signals. On-chip samplers offer, through the technique of repetitive sub-sampling a unique way to reconstruct signals without large loading [3]. A schematic of the set-up is given in figure 2a. A synchronization signal from the 82Mhz repetition rate Ti:sapphire laser is used to trigger a pulse-generator which in its turn is triggering the on-chip samplers. By measuring the output of the sampler at varying delays programmed in the pulse generator, we can reconstruct the repetitive signal at the input of the samplers.
Since the output of the samplers settles in a much smaller time-scale than the repetition period of the laser, we can use another sub-sampling device such as a digital oscilloscope to make multiple samples of the voltage at the input at one delay. By combining the statistics of these voltage uncertainties at different delays, we are able to deduce the timing uncertainty of the original signal.
Figure 2b shows the result of such a measurement. The samplers and receiver-less totem-pole are now implemented in a standard 0.25μm CMOS process. The flip-chip detectors on the device are $GaAs/Al_{0.3}Ga_{0.7}As$ multiple quantum-well (MQW) p-i-n diodes. The resulting graph is in fact a gray-scale image where, for given coordinates,

the intensity of a point is proportional to the probability of a sample, while the subplot shows the histogram of the measured rising edge crossing the 1.5V boundary.

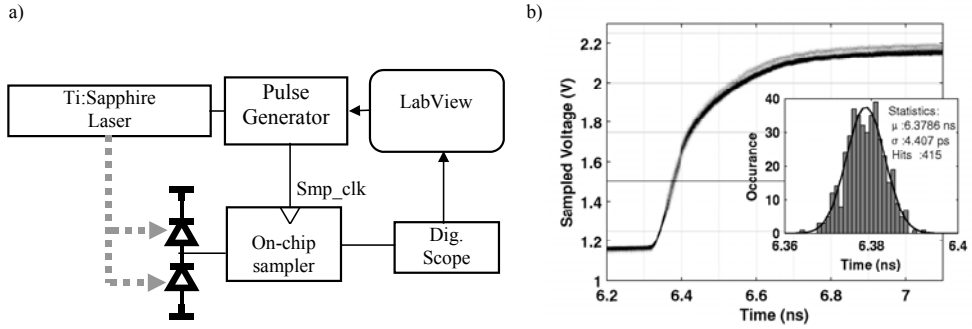

Figure 2: a) Schematic view of the set-up b) A jitter plot showing the result of the sampled rising edge of the MQW totem pole. The subplot shows the histogram of the signal at the 1.5V crossing point.

With this method we measure an rms-jitter of 4.4ps on the rising edge. This number matches well with the expected timing accuracy in the set-up. Indeed, directly measuring the optical pulse on a high-speed detector leads up to a 3.7ps rms-jitter when the scope is triggered with the pulse-generator. To demonstrate the noise-immunity of the approach, we compared the jitter between the receiver-less direct injection technique and the clock received by a conventional trans-impedance (TIA) asynchronous receiver. An uncorrelated 1Mhz square-wave was in the meanwhile superimposed on the supply with peak-to-peak values ranging from 0 to 150mV. The TIA-receiver showed a rms-jitter in the range of 11.0ps to 18.9ps for growing supply bounce. We have a smaller dependence on the supply noise for the receiver-less technique with rms-ijtter values ranging from 4.4ps to 5.3ps.

Modeling of an optical clock distribution tree.

We demonstrated the potential of direct receiver-less clock injection to deliver an accurate and power supply noise-tolerant clock at a single point on a chip. We now investigate the usability of this approach in a realistic clock distribution network in modern microprocessors.

We therefore model in this section at what depth in the clock distribution structure the introduction of optics would be more beneficial than conventional distribution networks. We investigate both the case of using receiver-less direct injection optical clock injection and the implementation of TIA-receivers.

The particular clock distribution network we are modeling is a symmetric distribution network consisting of inverter buffers which each drive four inverters in a balanced H-tree configuration targeting a 0.18μm technology. We include the wire-effects of the interconnection network, which will both add to the delay (RC-time delays)[4] and the electrical power consumption (more capacitance has to be switched and larger drivers are needed).

This clock distribution network, which is taken as a starting point, is being compared with an optical equivalent where to the top of the network has been replaced with optics. We define the optical insertion level as the number of inverters at the top of the distribution tree that are replaced by optics.

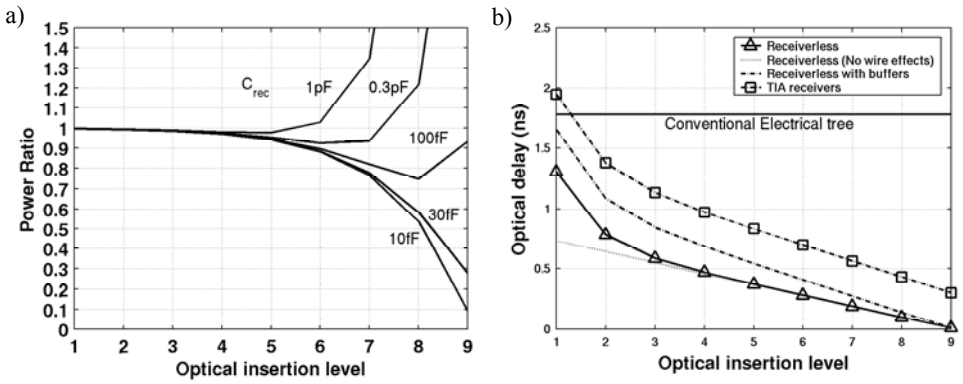

Figure 3: Modeling of the optical clock distribution a) The power consumed in the distribution tree and b) The total delay of the distribution

In figure 3 we show the results of the modeling of both the electrical power consumption and the delay for different levels of optical insertion. It is clear that only a small amount of power can be gained by introducing optics in the clock distribution. Even worse, when the capacitance of the optical detector or the power consumption in the receiver is large in comparison to the inverter capacitance, the required electrical power can even grow radically for optical insertion levels close to the latches. The gain in delay, and thus also the associated gain in jitter and skew, is much larger. For example an optical insertion at level 7 of this 9-level distribution tree would reduce the delay from 1.7ns to only 190ps, corresponding a 90% reduction.

Conclusion.

In this paper we have shown the potential of direct receiver-less optical injection onto p-i-n GaAs detectors. When a totem-pole of the detectors are optically driven by the stable pulse stream of a modelocked laser, well-defined sharp rising edges can be directly created on-chip, capable of driving small digital circuits. We experimentally demonstrated low-jitter receiver-less injection measured with on-chip samplers and showed that the technique is more noise-immune than a TIA-receiver implementation.
After demonstrating the potential of injecting the clock into one point on the chip, we modeled the usability of optical clocks for large distribution networks. Since most of the power is consumed in the last stage of a distribution network we found that the use of an optical clock will not make significant savings in the power consumption even if wire effects are included. However, the delay of the distribution can be significantly lowered in contrast. And hence large reduction in skew and jitter are possible.

References

[1] A.M. Braun, et al., “Universality of Mode-Locked Jiiter Performance”, IEEE Photonics Technology Letter, Vol 14, No. 8, August 2002

[2] Leaf A. Jiang et. Al, “Noise of Mode-Locked Semiconductor Lasers”, IEEE JSTQE, Vol 7, No 2 March/April 2001

[3] P. Larsson, C. Svensson, “Measuringhigh-bandwidth signals in CMOS circuis’, Electronics Letters, Vol 29, No 20, pp. 1761-1763, September 1993

[4] R. Ho, K. W. Mai, M.A. Horowitz, “The future of wires”, Proceeding of the IEEE, Vol. 89, No. 4, pp. 490-504, Apr. 2001.