Lab Test Bed Development for Evaluation of the GigaPON Uplink Performance

Zhe Lou, Stefaan Verschuere, Yanchun Yi, Dieter Verhulst, Xing-Zhi Qiu, Jan Vandewege

INTEC_design, Gent University,
St. Pietersnieuwstraat 41, B-9000, Gent, Belgium

A Lab Test Bed (LTB) that is aimed for evaluation of the burst-mode data transmission at 1.25Gbit/s speed over an upstream optical link is being developed and tested within the framework of the European project GIANT (GIgaPON Access NeTwork). It consists of a DSP board performing digital signal processing, communication and system control, 3 FPGA boards that are responsible for real-time operations and fast data exchanges, and physical layer high speed components under test such as upstream burst-mode transmitters and burst-mode receiver. This paper shows that the lab test bed is a generic and flexible test/control platform that can be used to evaluate various Physical Media Dependent (PMD) layer performances of advance point-to-multipoint gigabit optical access networks.

Introduction

A Gigabit-capable Passive Optical Network (GigaPON) system oriented for packet transmission is currently under development in the frame of European Project GIANT. Design and implement of 1.244Gbps packet transmission over a time division multiplexed Point-to-MultiPoint (P2MP) PON system is very challenging. The development efforts focus on the 1.244Gbps upstream burst-mode transmission with high performance, high transmission efficiency and cost-effective. The LTB is the first step towards the final GigaPON demonstrator. Its purpose is to have a platform on which we can test various critical PMD components and evaluate the PMD layer performance, especially the challenging GigaPON upstream subsystems.

The PMD components for 1.244Gbps upstream transmission mainly includes ONT (Optical Network Termination) Upstream burst-mode optical Transmitters (US-TX), and an OLT (Optical Line Termination) Upstream burst-mode optical Receiver (US-RX) including an APD TransImpedance Amplifier (APD-TIA) integrated module, a Burst-Mode Receiver (BM-RX) front-end and a Clock Phase Alignment (CPA) chip. Some of these devices are available from the Belgium IWT founded project SYMPATHI (SYMmetrical Pon AT HIgh bit rate), and some are still under development and/or fabrication. Therefore, two test scenarios of the LTB were made based on the availability of planned two GPON burst-mode chip sets.

In the early phase, the integration of the required PMD components and embedded real time software were realised and the PMD component performances were tested in terms of modulation speed, pulse waveform behaviour, duty-cycle distortion, burst mode receiver sensitivity, dynamic range and the RX run-in time. The results lead to validation of the PMD layer specifications and the requirements for the PMD layer components.

In a later test phase, more prospective lab tests will be performed on the LTB, to explore the possibilities and limitations of Gigabit TDMA upstream burst transmission with latest PMD components to be provided by SYMPATHI project, to verify Gigabit

upstream system concepts, particularly the Burst-mode BER (BBER), burst mode penalty, run-in behaviour, power budget and overall jitter. Test bed results allow enhancing the performance of the GigaPON demonstrator.
This paper will specify the architecture of the LTB and the 2 test scenarios.

System architecture and functionalities

The LTB mainly consists of a DSP board, 3 identical FPGA boards [1], 2 upstream transmitters (US-TX) and an upstream receiver (US-RX), as shown in figure 1.

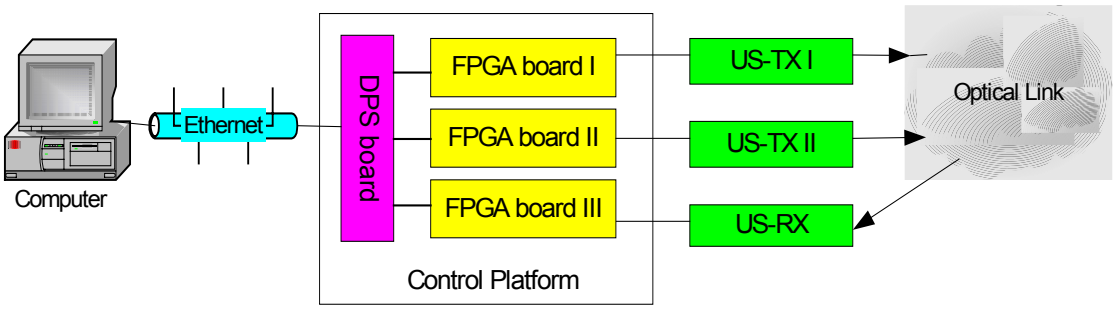

Figure 1. The system architecture of the LTB

- *The DSP board*

The DSP board is the main control unit that is responsible for data communication and system control. It has a built-in Ethernet connection that is used to establish the Internet connection. Therefore a Graphical User Interface (GUI) via network can control the LTB. The DSP board can program the 3 FPGA boards, so that the functionalities of these 3 FPGA boards can be modified without turning off the power. The data or commands sent via the GUI are processed in the DSP board before being sent to the FPGA board. Because of the speed limitation of the DSP processor, the DSP board does some non-time critical digital signal processing.

- *The FPGA board*

The FPGA boards are mainly used for high-speed data communication and real-time operations, e.g. Forward Error Correction (FEC). The Virtex-E series FPGAs from Xilinx are applied, which can drive/receiver 155Mbit/s 8-bit LVPECL data to/from US-TX/US-RX. It supports many I/O standards, including TTL, LVDS, LVPECL and CMOS. Since the I/O performance of some advanced FPGAs, e.g. Virtex-II, is increased to around 3Gbps by using source synchronous data transmission architecture, it is possible to upgrade the FPGA board to make a direct connection to the US-TX or US-RX without any glue logic.

- *Upstream transmitter and receiver*

The target boards to be tested are two US-TX's and a US-RX these are most critical GigaPON upstream PMD components/subsystems[2]. The key components are the 4 burst-mode GPON chips. Two process runs were planned. The purpose of the first version chip set is to prove the GPON system concept and verify some critical parameters. As the 1st phase chips contain only critical functions such as the full 1.244 Gbps data path, extra configuration/monitor functions have been implemented via the DSP board and the FPGA board to make the testing possible and emulate some functionalities that will be integrated into the second version chip set. Thus, it

requires some external circuits such as current sources, data and control signal interface besides the chip set on the TX/RX board. Moreover a fast but accurate Clock Phase Alignment (CPA) chip under development will also be integrated into the transmission link, which will communicate with the DSP board and the FPGA board for testing.

Test Scenarios

In order to fully evaluate the physical layer performance of the GigaPON upstream subsystem, 2 test scenarios were defined.

- *Test scenario I*

In the first test phase, only partly functional upstream transmitter (US-TX-Light) boards and upstream receiver (US-RX-Light) boards are available, so instruments have to be used for providing and/or receiving high speed and timing critical signals, due to the lack of full functional chips. Figure 2 illustrates the first test scenario in the LTB, where only one FPGA board was developed to control two US-TX Light boards.

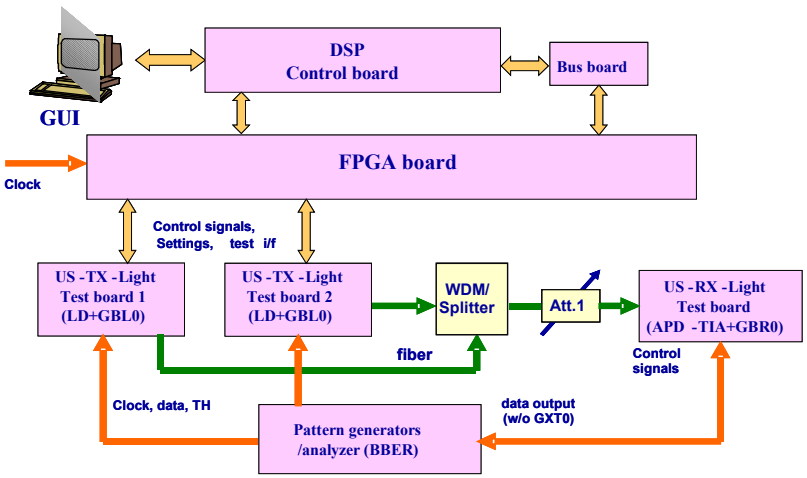

Figure 2. The realization of LTB test scenario I using the BBER tester

In the first test scenario, the DSP board and the FPGA board are mainly provided to offer some control signals to the US-TX-Light and US-RX-Light boards, e.g. setting the reference, bias and modulation currents, transferring the program data and implementing the slow APC control algorithm. The pattern generator provides the 1.244 Gbps data as inputs to the transmitters. And the data after processing by the receiver is fed back into the analyzer of the BBER test. This back-to-back uplink has been established and tested in the INTEC_design lab environment.

- *Test Scenario II*

In the first test scenario, since the data was generated from the pattern generator and fed back into the analyzer, it is difficult to include the upstream physical layer overhead and to generate the data payload with variable packet lengths (main. 15 bytes and max. 125 µs at 1.244 Gbps. Therefore an external multiplexer (MUX) board and demultiplexer (DEMUX) board as shown in Figure 4 have been developed; and will be integrated into the LTB during the test scenario II. This

configuration allows for the evaluation some important parameters and performance such as optimization of the distribution of the available bytes specified for the upstream physical layer overhead and some issues related to the GPON TC (Transmission Convergence) layer such as the employment of the FEC.

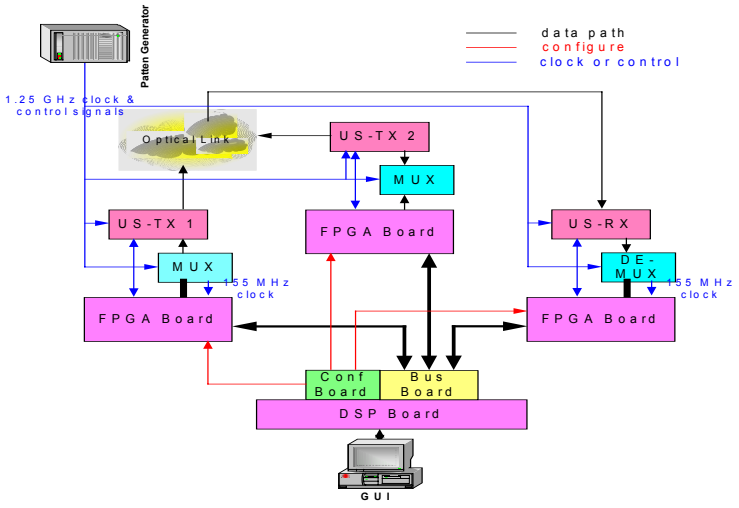

Figure 4. The LTB test scenario II with MUX/DEMUX boards

Instead of receiving data from the pattern generator, the US-TX boards will get data from a data file stored in the PC, which is going through the DSP board, FPGA board and MUX board. The FPGA board is not only doing some configuration, but also transmitting/receiving data to/from MUX/DEMUX boards. Based on this structure, FEC can be performed on the data by implementing FEC encoder and decoder in the FPGA board. Therefore the improvement of BER by applying the FEC can be evaluated in this setup.

Conclusion

This paper presents a lab test bed that is used to evaluate the physical layer performances of advance P2MP optical access networks. An embedded control platform, the DSP board plus the FPGA board, is applied for data communication and digital signal processing. Two test scenarios were defined and the test results we get now, shows it is a generic and flexible test bed for evaluation of the physical layer performance of the GigaPON upstream subsystem.

References

[1] Zhe Lou, Stefaan verschuere, Jo Pletincks, Xing-Zhi Qiu, Jan Vandewege, “A Java-Based Embedded Digital Signal Processing System”, will be published in the proceeding of WSEA conference, 2003.

[2] X.Z. Qiu, J. Vandewege et.al, “Burst mode transmission in PON access systems”, NOC’2002, Darmstadt, pp 127-132.