Alignment features for micro-optical interconnect modules

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Abstract

We report on the design, fabrication and characterization of micro-alignment features for a free-space multi-channel intra-chip micro-optical interconnect module. The features will be used for the alignment of the micro-optical module with respect to a 64x64 interleaved VCSEL/Detector array chip, ensuring the lateral and longitudinal alignment tolerances needed for high transmission efficiencies and low cross-talk on the optical channels. The features are fabricated with our in-house Deep Lithography with Protons technology. We also present our work on the characterization tools needed to assess the quality of the alignment features.

Introduction

The advances in chip technology, pushed by a never fulfilled hunger for computing power, fuels the growth of the transistor count in digital IC's. This evolution is still dictated by Moore's law but problems arise. The downscaling of the interconnect feature size deteriorates the signal quality and worsens the design complexity of the link. The wire dimensions are putting an aspect ratio limit to the bandwidth of the interconnections and advanced signaling techniques must be used to circumvent this physical limit[1]. Optics have been introduced as a "wire replacing technology"[2], and a lot of effort has been put in determining the potentialities of optical interconnects[3]. The trend for the introduction of optical interconnects in the lower levels of the interconnect hierarchy has been set, possibly reaching the on-chip interconnection level. The introduction of optics on this level is still under discussion and the outcome is uncertain. Despite this, we are investigating the use of free-space micro-optical interconnect modules (OIMs) to provide the proof-of-principle for on-chip interconnections. Recently, we demonstrated a 16 channel optical module with which we were able to interconnect 4 parallel channels on an opto-electronic field-programmable gate array[4]. The design rules and fabrication parameters for these components are well known now[5]. In this publication we present our preliminary efforts to bridge the last gap: the packaging of the OIMs.

After a brief introduction of the proposed OIM and the fabrication technology we use, we give an overview of the packaging issues. We report on the software tools we deployed for the analysis of microscope and profilometer data and present the results obtained up till now.

The FSOI module and fabrication technology

The micro-OIMs we design use micro-optical beam shaping and beam delivering structures[6], as shown in Figure 1, to interconnect emitters and detectors on the same chip via free space. A micro lens array collects and collimates the light coming from a

VCSEL array. As the light travels through the structure, it encounters a micro prism, which reflects the light back to the substrate. A second micro lens focuses the light onto the detector surface.

We use deep lithography with protons (DLP)[7], an in-house technology, to separately fabricate a micro lens arrays and a micro prisms. After assembly the resulting OIM can be used as a master to replicate the component using vacuumcasting[4,8].

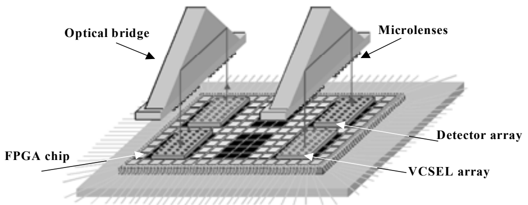

Figure 1: The concept of the OIM.

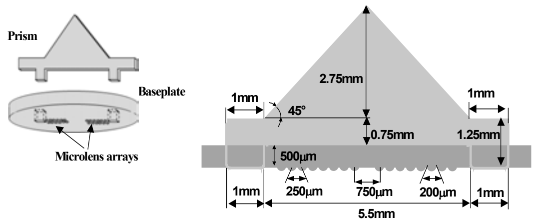

Figure 2: Typical dimensions of an OIM

The resulting OIM (see Figure 3) is a monolithic bloc in poly-urethane (PU) containing the micro lens arrays and the prism. An extensive study has been conducted in order to define the lens dimensions according to the system specifications and to establish the geometrical, dimensional and alignment tolerances[5].

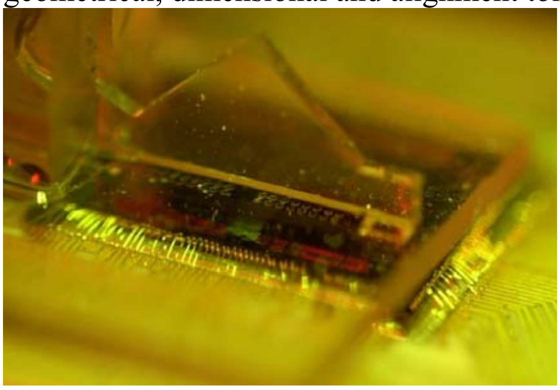

Figure 3: A side-view photograph of the replica of the 2x8 channel OIM aligned on an opto-electronic chip. This OIM has no interface structures with the chip package.

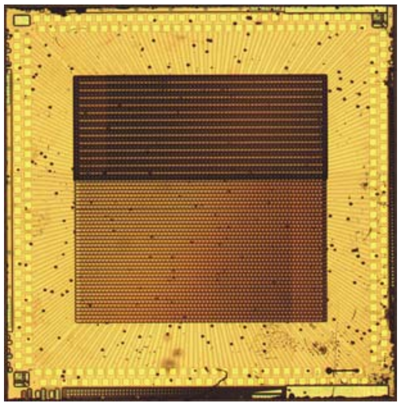

Figure 4: The targeted demonstration vehicle: a 64x64 interleaved VCSEL/Detector array chip.

Figure 4 depicts our new demonstration vehicle, containing 64x64 interleaved VCSEL/Detectors. The aim is to bring our OIM on top of this chip, using a dedicated pick and place alignment structure ensuring the accuracy to obtain flawless operation.

Packaging and characterization

Alignment is of course the main issue for the packaging of such components. Typical orders of magnitude for the lateral displacement and the longitudinal misalignment of the OIM above the chip are respectively ±2 µm and ±40 µm, or better. The spacer should keep the OIM at a working distance of several hundred µm above the chip. The tolerance stack-up of the individual interfacing structures will define if the above-mentioned constraints can be achieved. We refer to Figure 5 and Figure 6 depicting the working principle of a self-aligning structure with micro-balls which is under construction to study the stack-up of tolerances in a OIM package.

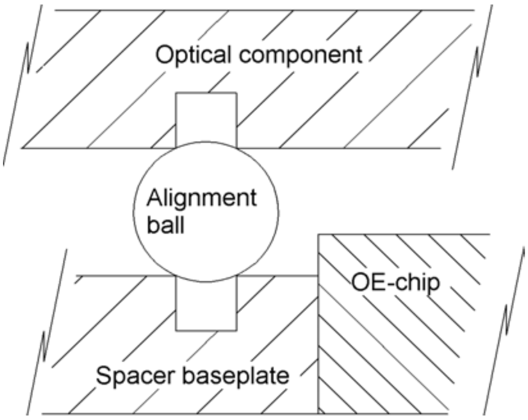

Figure 5: Self-aligning scheme with miniature steel balls.

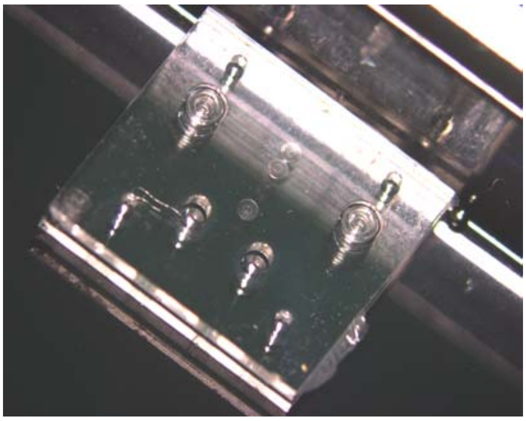

Figure 6: Test setup for steel ball alignment.

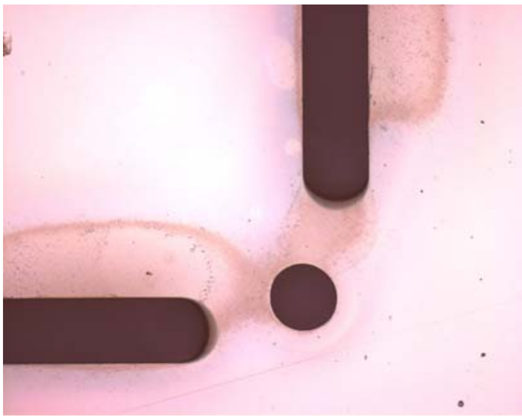

Figure 7: Typical test structure composed of 2 140 µm wide lines pointing to a 140 µm diameter hole (see also Figure 8).

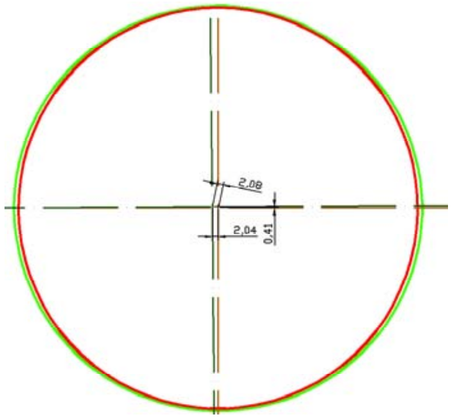

Figure 8: Design data (black) and resulting hole edges (gray). Errors are within numerical and measurement accuracies (values in µm).

In order to find the accuracy limits of our DLP process we fabricated several basic structures, such as the one in Figure 7. It consists of two 140 µm wide lines along the centerlines of a 140 µm diameter hole. Accurate measurement of the line coordinates and the hole center will give an indication of the positioning errors.
Another challenge is the accurate characterization of the components. High lateral as well as longitudinal resolution are desired over areas up to 5x5 mm. We used a WYKO non-contact optical profilometer, which is capable of measuring nanometer scale height differences, and have sub micron lateral resolution. We developed dedicated software to perform image analysis and measurement on the 3D data obtained from the WYKO instrument. This software enables us to fit edge and height data with elaborated models of different structures. Reverse engineering of the fabricated component is thus made possible, greatly enlarging the amount of detail with which we can compare design and fabricated structure (see Figure 8).

Results

Repeatable results were obtained with a 140 µm diameter beam. The resulting holes are slightly larger (142.8±0.2µm) and have a circularity of 98.9±0.8µm. We can guarantee a ±1 µm error on the line space between two parallel lines down to 10 µm space. The repeatability was demonstrated by fabricating exactly the same structures within a time

span of 4 months: we obtained slightly smaller hole diameters (141.3±0.4μm) with a higher standard deviation. The circularity also changed but is within the margins of the earlier measurements.
We simulated the behaviour of the steel ball alignment structure, taking the tolerances on the ball and hole geometries into account. We expected a nominal top height of 407 μm with a maximum of 412 μm whereas measurements revealed a height of 428±2 μm, which is still between the error margins for longitudinal alignment. The maximum deviation is lower than expected but we have a systematic offset of 11 μm with respect to the nominal value. We are currently investigating the cause of this error.
We observed a 2.1 μm lateral deviation for the structure of Figure 7. This error is merely a stack up of the measurement resolution and the numerical error of the image analyzer and highlights the need for large area high resolution measurements (<0.25 μm).

Conclusion

We designed and fabricated dedicated features to test the alignment of free-space optical interconnect modules. Our basic goal is the understanding of the dimensional tolerances achievable with the DLP process. We achieve a high degree of repeatability. The circularity of 140 μm holes is almost 99%. With dedicated optical characterization instrumentation and image analysis software we were able to reduce the measurement error down to the tolerance level we want to achieve with our components. Yet more research is needed to fully map all geometrical and dimensional tolerances of the DLP process.

References

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