Chip-to-chip parallel optical interconnects over optical backpanels based on arrays of multimode waveguides

Ronny Bockstaele (1), Michiel De Wilde (2), Wim Meeus (2), Hendrik Sergeant (1), Olivier Rits (1), Jan Van Campenhout (2), Johan De Baets (3), Peter Van Daele (1), Francois Dorgeuille (4), Sven Eitel (5), Michaela Klemenc (6), Richard Annen (7), Jan Van Koetsem (8), Jacques Goudeau (9), Baudouin Bareel (10), Reto Fries (11), Peter Straub (11), François Marion (12), Julien Routin (12) and Roel Baets (1)

(1)Department of Information Technology (INTEC), University Ghent, 9000 Gent, Belgium.

(2)Department of Electronics and Information systems (ELIS), University Ghent, 9000 Gent, Belgium.

(3)Department of Thin Films Component Group (TFCG), University Ghent, 9000 Gent, Belgium.

(4)Alcatel CIT, Marcoussis, France

(5)Avalon Photonics Ltd, 8048 Zurich, Switzerland

(6)Albis Optoelectronics, 8803 Rüschlikon, Switzerland

(7)Helix , 8008 Zurich, Switzerland

(8)FCI, s Hertogenbosch, Netherlands

(9)Nexans Research Centre, Lyon, France.

(10)Nexans Cabling System, Buizingen, Belgium

(11)PPC Electronics, Cham, Switzerland

(12)CEA-LETI, Grenoble, France

In the IO project, a demonstrator system consisting of optically connected computer boards plugged into an optical back panel is under development. On-chip optical access guarantees a compact, efficiency and cost-effective transmission of the digital data over optical fibre arrays. This paper will discuss the design and characterization of the IO optical interconnect demonstrator.

Introduction

Computer chips and systems are getting more and more powerful, due to advances in CMOS technology. Consequently, data rates between chips are growing. In current systems the data is transported over copper tracks on printed circuit boards and cables. However, as data rates continue to increase, data transport over copper cables gets more and more difficult. Current high-performance interconnects is based on 3.125 Gbps signaling over differential copper tracks. In such situation, the performance is limited by the electrical losses (skin effect and dielectric loss). A higher data-rate requires expensive low-loss dielectrics in the PCB. At that point, optical interconnects between chips will be preferred, because it offers important advantages. The signal loss in optical waveguides is much smaller compared to signal loss in copper tracks, and the data density (Gbps per square mm) can be much larger compared to electrical interconnects. Parallel optical interconnects is used today in high-performance computing systems for large (+/- 10 meter) distance interconnections, for example rack-to-rack interconnects. These modules are based on arrays of VCSELs and detectors. This technology is the best candidate for chip-to-chip interconnects. To bring this technology closer to the chip (to solve the interconnect bottleneck), novel technologies

need to be introduced: 2-dimensional arrays offer the multi-100-Gbps data access, a closer integration with the digital chips must be used (like flip-chipping), and the optical pathway should be integrated in the electronic boards. In the IST-IO project, a system demonstrator is build in which those challenges are studied and solved. This system includes optical backpanel, and digital chips with on-chip optical access. This paper gives an overview of the IO system demonstrator and the experimental results.

Description of the IO system

The IO demonstrator is a rack system with optically connected daughterboards. Digital CMOS chips in packages with integrated optical access are flip-chip mounted on the daughterboards, and an optical pathway is connected to these chips. The pathway includes chip connectors (coupling the optical pathway to the VCSELs and detectors on the chip), and backpanel connectors (coupling the waveguides in the daughterboard to the waveguides in the backpanel). Two 8x8 fibre arrays interface to the digital chip: one Tx (coupled to an 8x8 array with VCSELs) and one Rx (coupled to an 8x8 array with detectors).

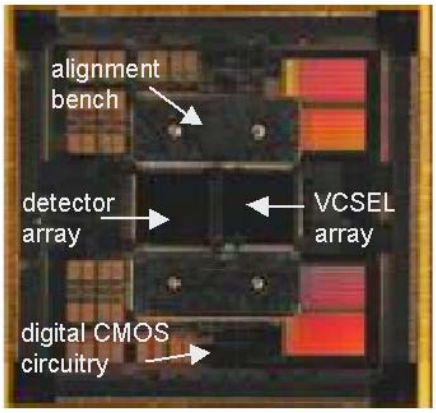

Figure 1: photo of the digital CMOS chip, with flip-chip mounted VCSELs and detectors and alignment structures

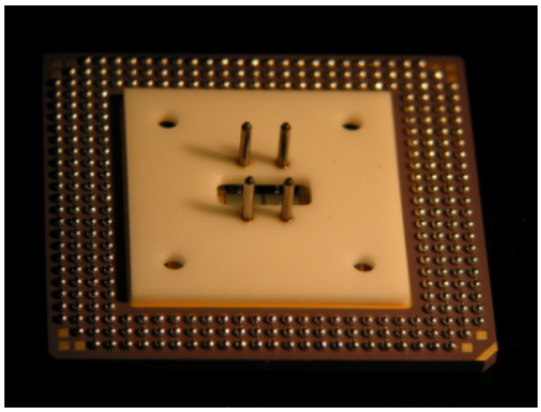

Figure 2: photo of finished BGA package, including the spacer plate with alignment pins

The laser transmitter and optical receiver are integrated in the package. The CMOS-integrated driver circuit converts the on-chip digital data in an analog current pulse, to drive the VCSEL. The CMOS-integrated receiver circuits convert the (small) analog detector current back into an on-chip digital data signal. In the project, circuits in 0.35um CMOS and 0.18um CMOS have been designed. The circuits are designed in a standard digital CMOS technology, and can therefore be integrated directly in any digital chip design, without the need for special analog chip technologies such as BiCMOS or SiGe. The optical link is based on 970-nm substrate-emitting VCSELs and backside-illuminated InP photodiodes. This device approach allows for a direct flip-chip attachment to CMOS chips. Uniform, efficient and fast (> 3GHz) components in 8x8 and 16x16 arrays have been realized. These opto components are directly mounted on the CMOS chip, using an indium solder reflow technique. Indium is a lead-free ductile solder, allowing for a high-yield and reliable hybridization. After the mounting on the CMOS chip, the opto components are mechanically thinned and an anti-reflection coating is applied to the backside of the VCSELs and detectors, to reduce optical absorption and reflection losses.

Two versions of optical pathways are developed in the project: a flexible pathway based on Plastic Optical Fibre (POF), and a stiff pathway based on glass sheets (which will can be integrated as and extra layer in printed circuit board stack). Multimode fibres (or waveguides) are used, with diameter around 60-80um. Compared to single-mode or free-space optics, the multimode fibre allows reducing the required alignment accuracy to ±10um. Dispersion limits of multimode fibres are not an issue, due to the rather short transmission distance (maximal a few meters). Plastic optical fibre has a smaller bending radius compared to glass fibres, allowing reducing the size of the connectors. Fibres based on novel low-loss polymers have been developed, and 1x8 fibre ribbons have been realized. Two types of optical connectors are developed. Backpanels connectors are integrated on the backpanel, and connect the daughterboard to the backpanel. The external dimensions are compatible with standard electrical backpanel connectors. The chip connector is the interface between the pathway and the chip (with opto-electronic components). Both connectors are based on MT-style ferrules with 8x8 fibres per ferrule. The fibre pitch in the ferrule is 250um, and the MT-style alignment pins are used to position the ferrule to the chip (or to the backpanel connector). The backpanel connector is based on a protruded ferrule: the fibre facet is protruded compared to the ferrule reference plane. The backpanel ferrule is a flat ferrule.

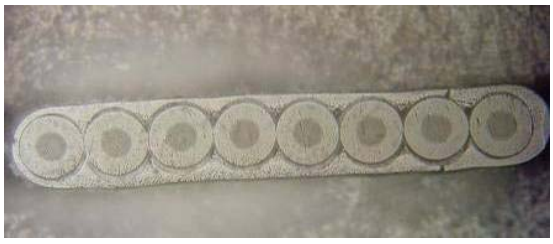

Figure 3 : 1x8 POF ribbon based on small-core, low-loss POF

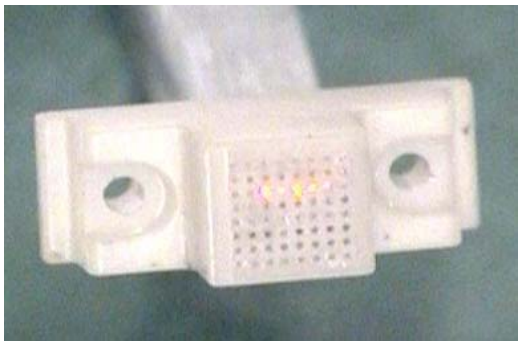

Figure 4: photograph of ferrule for chip connector, with POF fibres

The opto-electronic package contains the electronic chip (with the VCSELs and detectors), and accepts the chip connector. The chip is mounted in a dedicated ceramic BGA carrier. In a second step, a spacer plate with alignment pins is mounted on the package. This plate accepts the chip connector. Two approaches are used for mounting the spacer plate with the desired accuracy (in three dimensions!) on the ceramic package. In the first approach, micro-machined silicon parts determine the position of the spacer plate, which are flip-chip mounted on the CMOS chip. In the second approach, a contactless positioning technique based on coordinate measurement is used to position to spacer plate on the package. In a second version, the CMOS chip is flip-chip mounted on the ceramic carrier. This allows for a much smaller footprint, compatible with CSP (Chip Scale Package). In a last step, the package is mounted on the PCB with a standard PbSn solder reflow, and the optical pathway is insert

Experimental results

In the first experiment, a first-generation chip was mounted on the PCB. An optical loop-back connector was inserted on the package, connecting the 8x8 VCSEL array to

the 8x8 detector array on the same chip. Good functional links were achieved. Figure shows the measurement setup, with eye-diagram operating at 622 Mbps. A full working links was achieved with a VCSEL current of only 1.5mA, indicating that the coupling to/from the fibre is very good. Uniformity measurements are planned for the second-generation chips.
Figure shows the eye-diagram of the receiver part, as function of the transversal misalignment of the fibre. For large misalignment, the jitter in the receiver part increases fast, until the eye is completely closed.

Figure 5: measurement setup with loop-back connector on CMOS chip with optical access

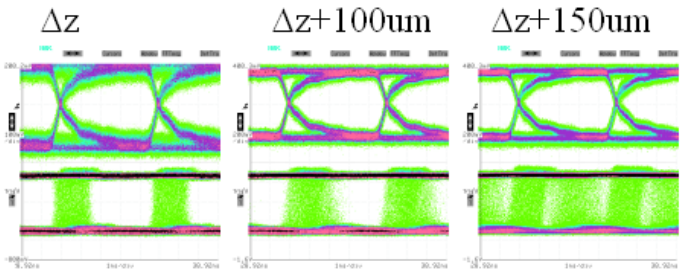

Figure 6: eye-diagram of external light source (upper trace) and detector-receiver combination (bottom trace) as function of distance from fibre facet to detector. Dz is 40um.

Conclusions

In spite of the progress of electrical interconnects, there is still interest to introduce parallel optical interconnects inside electronic systems, such as large computing systems. The advantages of parallel optical interconnects with on-chip optical access are clear: the optical loss in fibres is much smaller compared to the electrical loss in copper conductors, allowing for a much longer transmission length, or lower power dissipation. Furthermore, optics allows for a large data density, allowing for much large on-chip data access compared to electrical interconnects. Finally, optics results in simpler system (and PCB) design, due to the on-chip optical access. In this paper, the design, fabrication and characterization of the IO system demonstrator system were discussed. It is shown that the high-efficient chip-to-chip link can be fabricated, using manufacturable technologies.

Acknowledgements

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References

[1] Journal of Lightwave Technology, special issue on optical interconnects, vol. 22, NR 9, Sept. 2004.
[2] See http://www.intec.ugent.be/IO
[3] François Marion et al: “Packaging for Optical Rx/Tx Arrays: From BGA to CSP Packaging”, will be presented at IMAPS 2004, Long Beach, USA.