

# A compact detector for use in photonic interconnections on CMOS ICs

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*A possible solution for avoiding the bottleneck in the global interconnection of the future generation of CMOS ICs, is by adding an optical interconnect layer on top of the silicon electronic integrated circuits. We present a compact photodetector (PD) structure that can be used for such photonic interconnections and can be fabricated through wafer-scale processing. The PD is designed to detect the optical signal propagating in a waveguide layer on top of the CMOS. Light is coupled first to an InP membrane waveguide on top of the interconnect layer and is then absorbed and detected in the PD. Simulations have been performed to design and optimize the coupling and the PD structure.*

## Introduction

Future generation electronic integrated circuits (ICs) are expected to suffer a severe bottleneck in the global interconnect level, going towards smaller device dimensions and higher frequency regimes. A promising solution is given by adding an optical interconnect layer on top of the electronic silicon ICs, as it would provide bandwidth increasing and immunity to EM noise [1]. This interconnect layer is built as a passive optical wiring layer integrated with InP-based sources and detectors. Such work is carried out by the European project PICMOS<sup>3</sup>. In this project two possible integration techniques are studied, which assure compatibility towards future generation electronic ICs: a wafer-to-wafer bond technology and an above-IC approach [2, 3]. The optical wiring is realized by silicon-on-insulator (SOI) waveguides in the first integration approach and by or Si<sub>3</sub>N<sub>4</sub> waveguides in the second.

In this paper we present a compact photodetector structure that can be used for the above mentioned optical interconnections. The main difficulties in the design are achieving a good optical coupling from the photonic wiring layer to the PD and high quantum efficiency and electrical bandwidth. These key optical and electrical properties ideally require a different detector layout. Finding the optimum trade-off between them is then a challenge [4]. Simulations have been performed to design the PD and the results are described further in this paper.

## Photodetector design

A schematic representation of the PD structure is shown in Fig. 1. It is a pin-heterostructure,

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<sup>3</sup>Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), <http://picmos.intec.ugent.be>

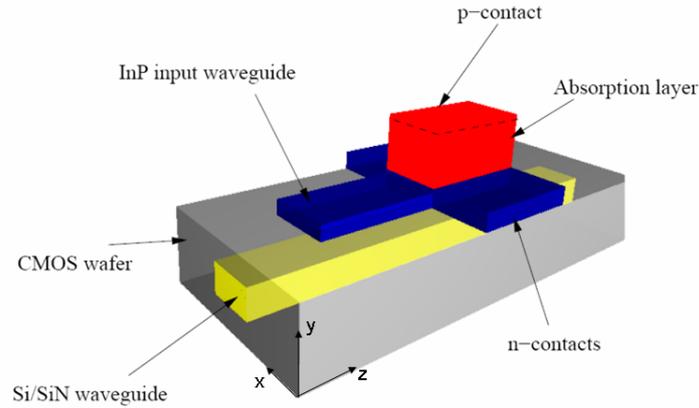


Figure 1: Photodetector structure. The coupling from the photonic wiring (Si/Si<sub>3</sub>N<sub>4</sub> waveguide) layer to the PD is realized by means of an InP membrane input waveguide. On top of it the detector is stacked and the optical power is detected in the absorption layer.

where an undoped InGaAs absorption layer is sandwiched between a p-doped InGaAs layer on top and an n-doped InP layer underneath. The photodiode structure is bonded on top of the interconnect layer where the optical signal propagates before entering the detector. Light is coupled first from the interconnect layer to an InP membrane waveguide, spaced by 300 nm (500 nm) when the photonic wire is realized in Si (Si<sub>3</sub>N<sub>4</sub>), then it is absorbed and detected in the PD.

Simulations have been performed to design the input passive waveguide and the layer stack of the PD. According to the coupled-mode theory, to optimize the coupling between waveguides, the propagation constants of the modes guided by the waveguides should be the same (mode-matching condition). The coupling efficiency  $\eta_c$  is defined as

$$\eta_c = \frac{c^2}{c^2 + (\Delta\beta/2)^2} \cdot \sin^2 \left( (c^2 + (\Delta\beta/2)^2)^{\frac{1}{2}} \cdot z \right) \cdot e^{-\alpha z},$$

where  $c$  is the coupling coefficient,  $\beta$  the mode propagation constant,  $z$  the field propagation direction and  $\alpha$  the loss factor [4]. The value of  $\eta_c$  is maximum when the propagation constants of the modes are the same ( $\Delta\beta = 0$ ). A 2D Finite Difference mode solver<sup>4</sup> has been used to calculate the mode propagation constants. The simulations have been performed choosing a certain thickness for the InP waveguide and sweeping its width. Because of the high refractive index contrast of the materials involved, mode-matched InP waveguides will be very small. Thus the InP waveguide thickness has been chosen as small as possible in order to avoid widths too small for current lithography technology and for further processing after the waveguide lithography. For optimum coupling, we have chosen InP waveguide thickness (width) values of 0.25  $\mu\text{m}$  (1  $\mu\text{m}$ ) and 0.2  $\mu\text{m}$  (0.34  $\mu\text{m}$ ) for coupling from Si and Si<sub>3</sub>N<sub>4</sub> waveguides, respectively (see Fig. 2). The coupling length is calculated to be 13  $\mu\text{m}$  and 12  $\mu\text{m}$  for Si and Si<sub>3</sub>N<sub>4</sub>, respectively. Fig. 2 also shows that fabrication tolerances for the InP waveguide are critical in both cases. A lateral taper in the coupling InP waveguide can be used to increase the fabrication tolerances.

The PD layer stack must be designed in order to maximize the coupling from the input InP waveguide to the detector absorption layer. This way the largest portion of the optical

<sup>4</sup>“Selene”, commercial software by C2V (<http://www.c2v.nl>)

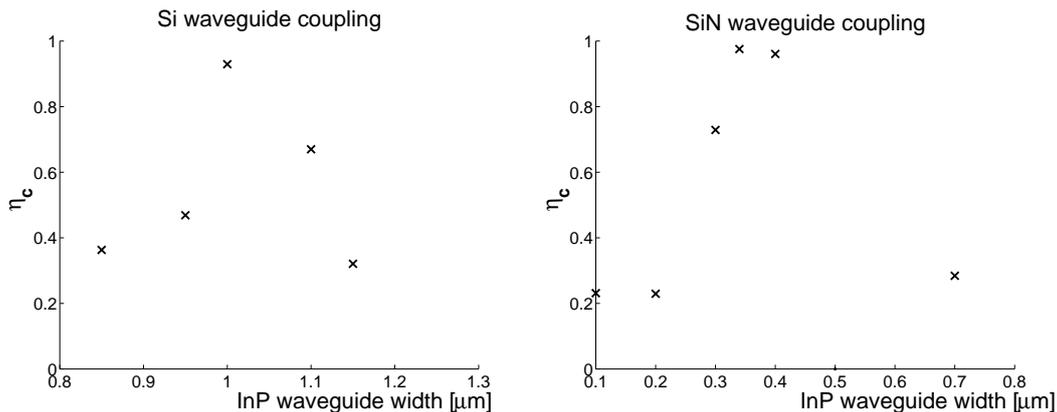


Figure 2: Coupling efficiency versus InP input waveguide width. InP waveguide thickness values are  $0.25\mu\text{m}$  and  $0.2\mu\text{m}$  for Si and  $\text{Si}_3\text{N}_4$ , respectively.

power is detected and the quantum efficiency is maximized. Optimization of the optical properties can be achieved by increasing for instance the absorption layer thickness. However that would result in a degradation of electrical figures, like the bandwidth, as the carrier transit time would increase [4]. Simulations have been performed to investigate the optimum design of the PD, as a function of the layer thicknesses, for maximizing the optical features. The PD structure we have chosen is a pin structure made of an undoped  $700\text{nm}$  InGaAs absorption layer cladded between a  $50\text{nm}$  highly p-doped InGaAs contact layer and a highly n-doped InP layer. The last layer is also used to realize the input waveguide. The device we present in this paper can be very compact, with a footprint as small as  $50\mu\text{m}^2$ . Simulations show that for such a detector more than 90% of the optical power is absorbed within  $7\mu\text{m}$ , as can be seen in Fig. 3, where the optical power absorption for InGaAs is taken to be  $\alpha = 0.7\mu\text{m}^{-1}$  at  $\lambda = 1.55\mu\text{m}$ . However, part of the power is absorbed in the p-doped contact layer and in the metal layer. The light absorbed in this region is lost, as it does not contribute to the generated photocurrent. Taking this into account, our simulations indicate that the internal quantum efficiency will be over 70%. The 3-dB electrical bandwidth of the detector is mainly limited by the RC-time and by the carrier transit time in the depletion region [5]. The capacitance can be calculated as

$$C_j = \frac{\epsilon_0 \epsilon_r A}{w_{\text{dep}}},$$

where  $\epsilon_r$  and  $w_{\text{dep}}$  are the permittivity and the thickness of the depletion layer and  $A$  the mesa surface [6, 7]. This takes only the detector mesa into account and not parasitic effects like the probe pad capacitance. Substitution of the values leads to a capacitance of 9 fF. The series resistance  $R_s$  is found considering the contributions of the resistances at the metal-semiconductor interface, for both p-side ( $R_p$ ) and n-side ( $R_n$ ). They are calculated as

$$R_p = \frac{\rho_c}{A} \quad \text{and} \quad R_n = \frac{1}{2} \cdot \frac{d_n}{q\mu_n N_d w_n L_{\text{PD}}},$$

where  $\rho_c$  is the specific contact resistance of the metal-semiconductor interface,  $d_n$  the distance from the middle of the detector to the n-contact,  $w_n$  the thickness of the n-doped layer,  $L_{\text{PD}}$  the length of the detector and  $\mu_n$  the mobility of the electrons [8]. Using values from previous experiments [8], we calculate  $R_p = 10\Omega$  and  $R_n = 8\Omega$ . Considering

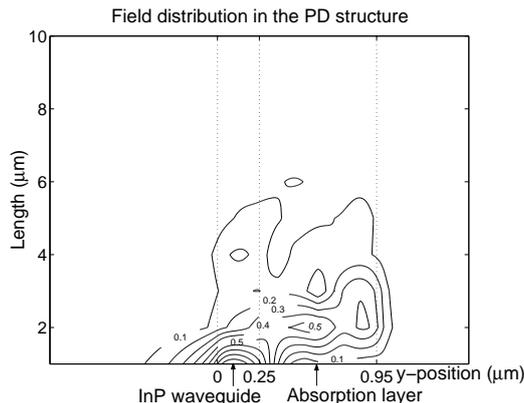


Figure 3: Simulations on PD length. The field distribution after the interface between the input waveguide and the detector is plot. Light propagating in the InP waveguide is coupled into the depletion layer of the PD. More than 90% of the power is absorbed within  $7\mu\text{m}$ .

a load resistance of  $50\Omega$ , the RC-time  $\tau_{\text{RC}}$  and the transit time  $\tau_{\text{tr}}$  are calculated to be 10 ps and 40 ps, respectively. The 3-dB electrical bandwidth can then be calculated as  $\frac{1}{f_{3\text{dB}}^2} = \tau_{\text{RC}}^2 + \tau_{\text{tr}}^2$  which leads to a speed of 24 GHz.

## Conclusions and acknowledgement

We presented the design of a photodetector structure suitable for integration on an optical interconnect layer on top of CMOS electronic circuits. The device has a 700 nm InGaAs absorption layer and a footprint of  $50\mu\text{m}^2$ . Simulations were performed to design the detector and predict its performance. It is shown that for compact devices a 3 dB electrical bandwidth of 24 GHz can be achieved with an internal quantum efficiency of more than 70%.

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