A Novel Automotive VCSEL Driver with Feed-Forward Bias and Modulation Current Control

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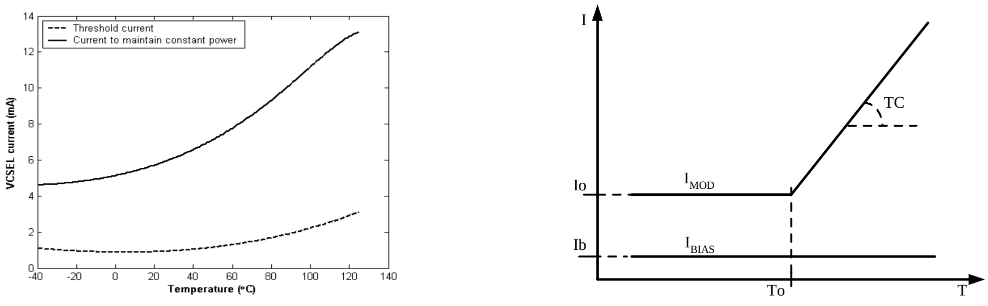
Abstract – We propose a novel 50 Mb/s optical transmitter fabricated in 0.6 μm BiCMOS process for automotive applications. The proposed VCSEL driver chip was designed to operate from a single supply voltage ranging from 3.0 V till 5.25 V. A novel internal feed-forward current control circuit is presented to stabilize the emitting light power without any external components. The experimental results show that the output light power can be trimmed within a 1.5 dB range over the automotive environmental temperature range of –40°C till 105°C.

Introduction

In this paper, we address the design of a VCSEL driver that is intended for automotive applications. The main difficulty in the automotive environment to be overcome is the requirement over a wide environmental temperature range, i.e. from –40°C till +105°C. On top of this, the chip was required to operate with a very wide supply voltage range, from 3.0 V till 5.25 V. The optical transmitter, consisting of the driver and the VCSEL is required to emit stable optical output power with narrow tolerance. Traditional laser drivers employ a photodiode that is coupled to one of the backfacets of the laser diode to monitor the optical output power forming an automatic power control (APC) loop. Unfortunately, typically a VCSEL does not posses such a backfacet photodiode, making the use of a feedback loop very difficult. Ordinary feed-forward (open-loop) control, however, includes a variable resistor off the chip [1]. It needs an additional pin and is not cost-effective. Therefore, pure on-chip feedforward compensation of the temperature dependence and calibration of the process dependence was used here to stabilize the optical output power of the VCSEL.

Transmitter Architecture

Fig.1 shows the required current needed to bias the VCSEL to ensure constant optical output power. As can be seen, this curve can be approximated by a piecewise linear function. In our feedforward compensation scheme, the following method was proposed. First, the bias current (i.e. the fixed current transmitted when a digital ‘0’ is transmitted) is kept constant with temperature, and characterized by the parameter *Ib*. The modulation current (i.e. the difference in applied current between transmission of a ‘1’ and a ‘0’) can be characterized by the initial value *Io*, the threshold temperature *To* and the temperature coefficient *TC* of the modulation current. These four parameters must be chosen differently for each VCSEL, and also depend upon the process corner of each chip. To maintain constant optical output power, these parameters are therefore digitally adjustable via zap cells, which are set during a calibration step.



(a) (b)

Fig. 1. (a) Typical VCSEL current versus junction temperature (b) Proposed feedforward control for bias and modulation current

The architecture of the transmitter is shown in Fig. 2. It mainly consists of a buffer that converts a single-ended input to a differential signal, that in turns is used to control the driver itself. Using zapping circuits, the currents generator can be adjusted to match the silicon and VCSEL process corners.

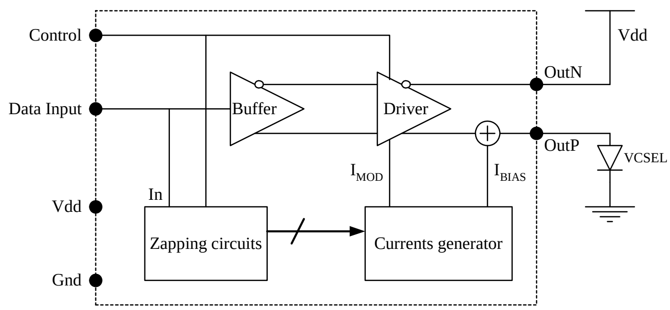


Fig. 2. Transmitter architecture

Circuit Description

VCSEL output driver

To reduce costs, no external ac-coupling capacitance can be used in this design. Therefore, the VCSEL is dc-coupled to the driver. Of major concern for any dc-coupled laser or VCSEL driver is the headroom left at the smallest supply voltage (3V) to drive the VCSEL. Here, this problem was solved by employing the common cathode configuration [2], using the threshold voltage of the VCSEL itself to bias the collector voltage of the differential pair.

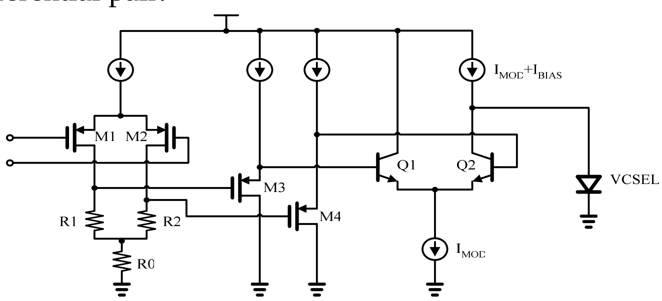


Fig. 3. Schematic of the VCSEL driver

A major problem in this design is the fact that the input common-mode voltage of the input buffer is referred to the supply voltage, which ranges from 3.0 V till 5.25 V. Hence, given the associated wide common-mode swing, this signal cannot be directly applied to the differential output pair. Therefore, we used a pMOS differential pair (M1,M2) to refer the common-mode voltage to ground. The common-mode voltage is now determined by the tail current of the pMOS differential pair (M1,M2) and level shifters M3 and M4.

Bias current generator

Using an on-chip bandgap reference, one can easily produce a voltage that shows little dependence upon temperature and process corners. Typically, one then generates a precision current using this bandgap voltage and an external precision resistor. However, this requires an additional I/O pin, which is not available. As the absolute value of an on-chip resistor varies a lot with process corners (about ±20%), any current derived from a bandgap voltage and an on-chip resistor has the same process dependency as this resistor.

As these process variations result in unacceptable tolerances on the emitted optical output power, they will be removed via a calibration procedure. As shown in Fig. 4 first removes the process dependency by using the process calibration cell,

$$I_{cal} = I_0 + Cal<1>\cdot I_1 + ... + Cal<8>\cdot I_8$$
$$= (k_0 + Cal<1>\cdot k_1 + ... + Cal<8>\cdot k_8)\cdot I_{in} = K_{Cal}\cdot I_{in}$$

where *Cal<1:8>* is an 8-bit calibration value, which can be set by the zapping circuits, and $k_0 \dots k_8$ is the current mirror ratio of each branch. By setting the calibration value and ratios of the current mirror (so the ratio K_{Cal}), we can calibrate the output reference current to a process-independent value. After the process calibration, another stage of calibration cell with different current ratios is used for setting the *Ibias* parameter for the bias current. The final output bias current is $I_{BIAS} = K_{Ibias}\cdot I_{Cal} = K_{Ibias}\cdot K_{Cal}\cdot I_{CONST}$.

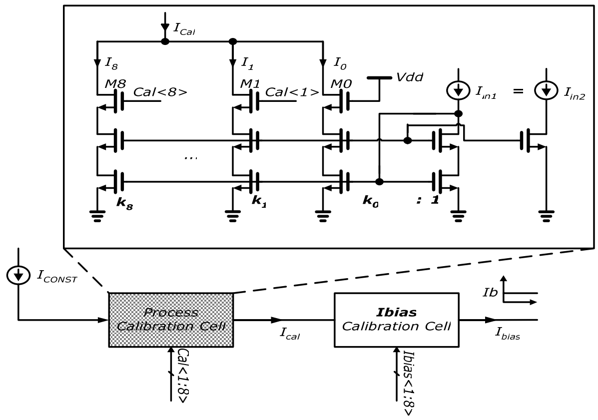


Fig. 4. Schematic of bias current generation

Modulation current generator

The schematic diagram of modulation current generator is shown in Fig. 5. The circuit is composed of two branches of current generators - I_{upper} one and I_{lower} one. The lower branch, which set *Io* of the modulation current, has similar structure as the bias current generator. The upper branch generates the current with desired *To* and *TC* settings. The first step is to introduce *To* cross-point into I_{upper} current. This is carried out by subtracting calibrated current constant to temperature (I_{CONST}) from proportional-to-absolute-temperature current (I_{PTAT}) via current mirrors. The output I_{To} is given as,

$$I_{To} = \begin{cases} K_3\cdot(K_2\cdot I_{PTAT} - K_1\cdot K_{To}\cdot I_{CONST}), & if\ T \geq T_0 \\ 0 & ,\ otherwise \end{cases}$$

where *To* is the temperature point that makes $K_2\cdot I_{PTAT} = K_1\cdot K_{To}\cdot I_{CONST}$. Because the I_{PTAT} and I_{CONST} have the same process dependence, the resulting zero cross-point *To* is only dependent on K_{To} in the first order. I_{To} is then calibrated with process calibration cell and TC calibration cell is used to set the temperature coefficient of the modulation current. Finally the upper and lower currents are added together to form the modulation current.

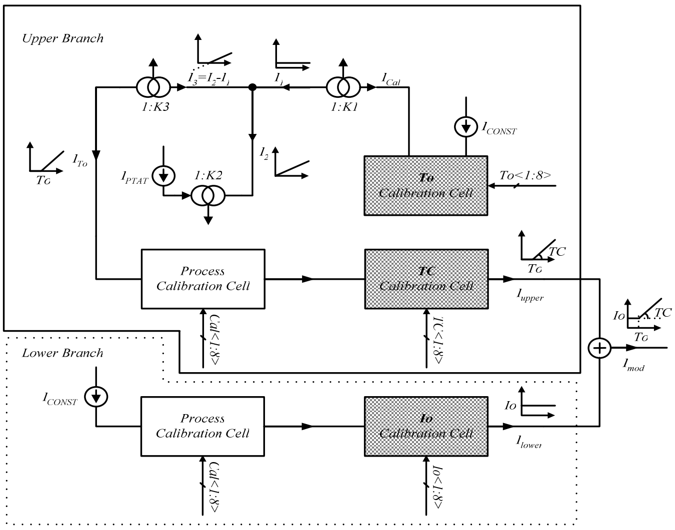
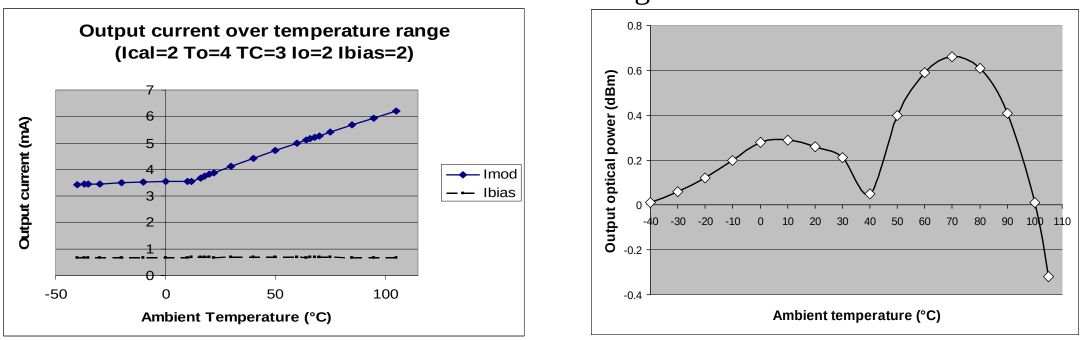


Fig. 5. Schematic of modulation current generation

Experimental Results

The VCSEL driver was designed on the base of the XFAB 0.6um BiCMOS process. The driver was put into the temperature chamber and the output currents and optical power were measured. The results are shown in Fig. 6.



(a) (b)

Fig. 6. (a) Measured bias and modulation currents versus temperature (b) measured output optical power versus temperature

As shown in Fig. 6.(a) the bias and modulation current was properly generated by the internal current generator. And it is obvious from Fig. 6.(b) that the feed-forward temperature compensation scheme works very well and output power varied within 1.5 dB over the temperature range from -40 to 105 °C.

Acknowledgement

The work was partly supported by the Flemish Government under the research contract IWT AutoFUN and partly by Melexis.

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