Deep etching of DBR gratings in InP using Cl_2 based ICP processes

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We present the progress on deep etching of InP for the fabrication of DBR gratings in Photonic Integrated Circuits (PICs). Various etching chemistries were investigated using an Inductively Coupled Plasma (ICP) etching system. It is shown how the different process settings determine the etched profile and sidewall roughness. Different masking techniques were also investigated. Hard masks using SiN_x and SiO_2 layers are discussed, as well as a three-level masking technique using hard baked photoresist or polyimide. Special attention is paid to applying Electron Beam Lithography (EBL) in the fabrication of the etching mask. A combination of Aluminum lift-off and SiO_2 shows the best results.

Introduction

Dry etching processes are widely used in the fabrication of Photonic Integrated Circuits (PICs) in InP. New devices like Distributed Bragg Reflector (DBR) gratings and photonic crystal structures demand deep etching processes that are able to etch high aspect ratio trenches and mesas with straight and smooth sidewalls [1][2]. But also deep etched waveguides are interesting applications because the increased lateral contrast allows smaller devices and thus the possibility to integrate more devices on a single chip. Side wall roughness is one of the key parameters for this application.

An Inductively Coupled Plasma (ICP) machine is one of the most suitable etching systems for fabricating deep (>2 um) and high aspect ratio structures. In such a system the plasma is generated using a separate induction coil which enables the user to control the ion density (ICP power) separately from the ion energy (RF power). This allows a better process flexibility.

The quality of the etched structures depends very much on the chemistry of the etching gasses. Several chemistries are possible, but in this paper we will concentrate on chlorine based processes. We will discuss a pure Cl_2 process, a Cl_2-CH_4-H_2 process and a Cl_2-Ar-H_2 process. Each process has its advantages and disadvantages.

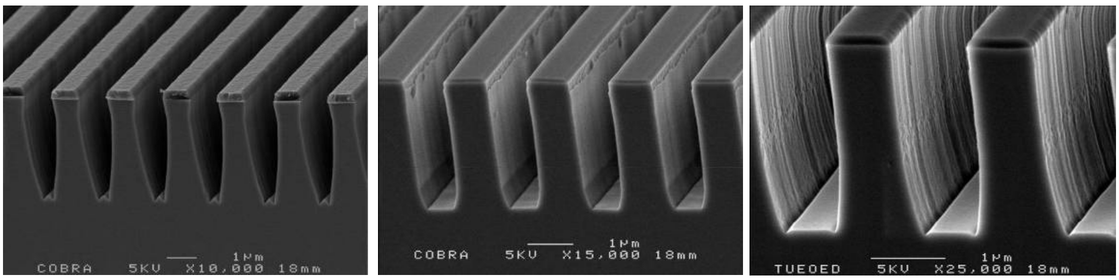
The sidewall roughness is not only depending on the ICP etching process, but also on the used mask. In general, when using high power ICP processes, we need a thick mask with a good selectivity with respect to InP. But we must also keep in mind that the dimensions of the structures are becoming smaller and smaller and feature sizes are already well below 1 um. This means that the mask must be fabricated using Electron Beam Lithography (EBL). Three different EBL masking techniques will be discussed, 1) direct E-beam writing in ZEP e-beam resist on a SiN mask, 2) a three level process with a hard-baked photoresist buffer layer and 3) an aluminium lift-off process using PMMA e-beam resist on SiO_2.

Etching chemistries

Most etching process used in ICP etching of InP are based on chlorine. The Cl_2 ions react with the indium and phosphide atoms creating $InCl_3$ and PCl_3 and PCl_5 atoms, which are quite volatile under low process conditions. However, if the process temperature is too low (<150 ºC) the $InCl_3$ tends to induce micro-masking that results in rough etched surfaces [3].

The simplest process to etch InP is to use a pure chlorine plasma. This chemistry results in very smooth surfaces and the selectivity of the InP with respect to the etching mask (SiO_2 or SiN_x are suitable materials) is usually more than 20:1. However, etch rates are generally low (< 1 µm/min) and the shape of the etched structures tends to be smaller at the bottom. This shape can be improved slightly by adjusting the process pressure and the gas flow, but it can never be completely straight. Although this is a problem for high aspect ratio structures with very narrow openings, for deep etched waveguides a wider waveguide foot is not a big problem, because the waveguide film is usually less than 2 µm below the top of the waveguide.

To increase the etch rate and improve the directionality of the etching process, some argon can be added to the process chamber. The argon ion bombardment adds energy to the etching process. This increases the etch rate and improves the etched profile. However, the argon also causes the mask to degrade quicker. Some faceting on the corners of the mask is observed and if the etch time is too long, this faceting will cause extra roughness on the etched sidewalls.



Cl_2 | Cl_2-Ar-H_2 | Cl_2-CH_4-H_2

Figure 1: Different etching chemistries result in different etch profiles

Adding hydrogen to the chemistry results in some passivation of the etched surface. It decreases the under etch and results in smoother sidewalls. The ratio between Cl_2 and H_2 should be chosen carefully. The best results were obtained using a Cl_2:Ar:H_2 ratio of 7:4:12 sccm and a pressure of 4 mTorr.

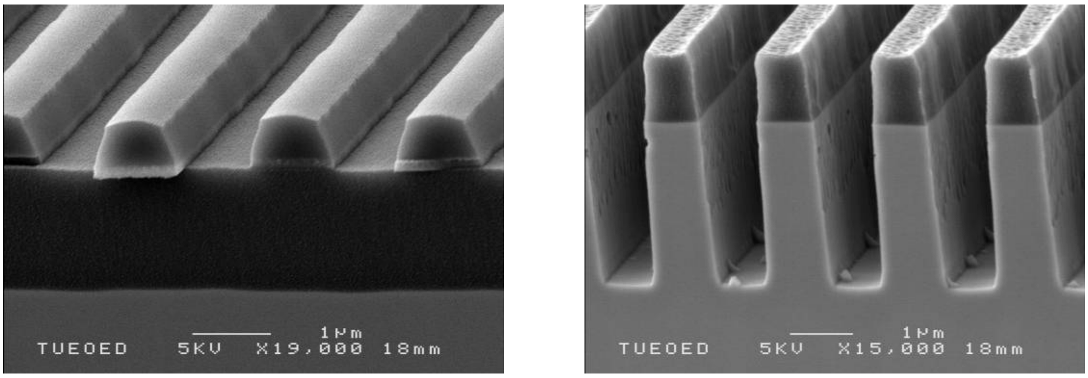
Another way to passivate the sidewalls of the waveguides, and thus to decrease the roughness, is to add some methane to the process. The CH_4 creates a polymer coating that protects the sidewall to further etching by the Cl_2 species. This results in smoother sidewalls and lower waveguide losses [4]. However, etch rates are also lower, while mask erosion is more or less the same as in the Cl_2:Ar:H_2 case. The roughness visible in fig. 1 is mostly caused by this mask erosion. The optimal gas flow was found to be Cl_2:CH_4:H_2 7:8:5.5 sccm and 4 mTorr process pressure.

2-level masks using SiN_x

The conclusion of the investigation of the different chemistries is that there are different ways to improve the sidewall roughness by adding passivating species. However, the passivation also brings down the etch rate. This means that to obtain a deep etch, a thicker mask is required. In most dry etching processes it is common to use SiN_x or SiO_2 as etching mask, because photoresist does not withstand the plasma sufficiently. The SiN_x or SiO_2 is opened with photoresist as a mask. However, in the case of electron beam lithography (EBL), the resist layer thickness is limited. In a 30 kV EBL system the maximum thickness in which small structures can be defined with enough accuracy is about 300 nm. This limits the thickness of the SiN_x or SiO_2 to about 400 nm, although thinner masks give better results (less roughness).

3-level masks

Another way of making thick masks is using a 3-level masking method, instead of the 2-level method described before. In this method, first a thick layer (~ 1.5 µm) of photoresist or polyimide is spun on the InP, which is completely hard-baked. Next a thin layer (~100 nm) of SiO_2 is deposited on the hard-baked resist. This thin SiO_2 can then be opened by RIE using an EBL pattern. In the next step the hard-baked resist is opened with an O_2:Ar plasma in the ICP machine. The result is a thick high aspect ratio photoresist mask that can be used for further ICP etching of the InP.



InP substrate – hard baked resist – SiO_2 – photo resist

Trenches in InP with hard baked resist as a mask

Figure 2: SEM photographs of the 3-level mask method

The main problem with this etching process is that the hard baked resist does not withstand elevated temperatures. Especially very small structures have this problem. But, as mentioned before, a certain temperature is needed to make sure that all the etch species are removed, so this is a difficult trade-off. Also the lateral etching is higher than in the case of SiN_x or SiO_2 hard masks.

Aluminium lift-off on SiO_2

Another approach to obtain thick masks is to find an alternative to open a thick SiN_x or SiO_2 layer. These materials are usually etched in an RIE system using a CHF_3 plasma, but the standard resists are not sufficiently thick to withstand long etching times. However, there is some good experience using titanium as a mask to open SiN_x layers

[5] and using aluminium has an even higher selectivity with respect to SiO_2 in a CHF_3 chemistry.
The process that was developed using aluminium as a mask is as follows: First a 530 nm layer of SiO_2 is deposited by PECVD and then a 200 nm layer of PMMA 950K A4 EBL resist was spun on the sample. The sample is exposed at a relatively low acceleration voltage of 20 kV, which increases the forward scattering of the electrons in the resist. This causes a slight undercut in the resist profile, which is necessary for the lift-off process. After development a 70 nm layer of aluminium is deposited by electron beam evaporation. Then the PMMA is removed by acetone and the exposed structure remains as an aluminium mask. The SiO_2 mask is then opened in a CHF_3 RIE process which is then used as an etch mask in a Cl_2:Ar:H_2 ICP process.

In fig. 3 two 1 µm wide waveguides are shown. One with a DBR grating that goes through the whole waveguide and one with a grating depth of 50 nm. The etch depth is 3.9 µm and the etched sidewalls are very steep. The side wall roughness is caused by the roughness of the aluminium mask. To improve this roughness we need to optimize the aluminium thickness and the deposition process.

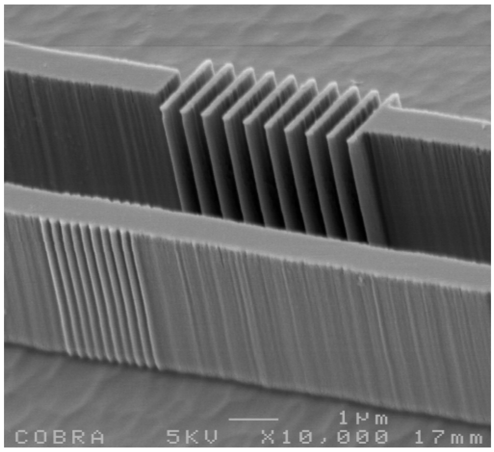


Figure 3: SEM photograph of DBR gratings in 1 µm wide waveguides

Conclusion

To obtain high aspect ratio structures, the chemistry of the etching process is very important. A Cl_2:Ar:H_2 chemistry gives the most vertical sidewalls, but requires very thick masks. The fabrication of these thick masks is difficult, especially using a low voltage EBL system. A process using a 70 nm aluminium lift-off process on top of a 530 nm SiO_2 layer allows us to etch 3.9 µm deep with high aspect ratio. This process seems very promising for the fabrication of DBR gratings and other sub-micron, deep-etched structures like photonic crystals.

References

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