Membrane couplers and photodetectors for optical interconnections on CMOS ICs

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We introduce a compact photodetector (PD) suitable for photonic interconnections on silicon ICs. In such applications, the optical sources and detectors are linked via waveguides in an interconnection layer which is on top of CMOS circuitry. The photonic devices are fabricated with wafer scale processing steps, guaranteeing compatibility towards future generation electronic IC processing.

In our approach, the optical signals propagating through the waveguides in the interconnection layer are coupled into the PDs via InP membrane waveguides. These coupling structures were designed using 3D modal analysis. Device simulation and fabrication are described in this paper.

Introduction

For future generation electronic ICs, a bottleneck is expected at the interconnect level. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution, providing bandwidth increase, immunity to EM noise and reduction in power consumption [1, 2]. This solution is investigated within the European project PICMOS[6]. In that context, the interconnect layer is built as a passive Si optical wiring layer and the InP based photonic sources and detectors are fabricated with wafer scale processing steps [3]. A possible integration technique, which assures compatibility towards future generation electronic ICs, is based on a die-to-wafer bonding technology [4, 5].

In this paper we present a compact photodetector structure that can be used for the above mentioned optical interconnections. One of the main difficulties in the detector design is achieving a good optical coupling from the photonic wiring layer to the PD. In our structure, an InP membrane waveguide is used to couple the optical signal out of the Si wiring layer. Coupler design and fabrication are described further in this paper.

Detector design

In our approach, the optical coupling from the photonic wiring layer to the PD is realized via an InP membrane input waveguide on top of a SiO_2 bonding layer, like shown

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[6]Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), http://picmos.intec.ugent.be

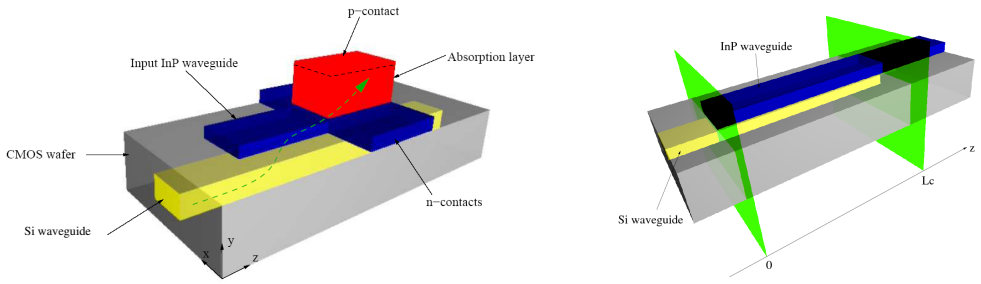

Figure 1: Photodetector structure (left): the dashed arrow indicates how the coupling from the photonic wiring (Si waveguide) layer to the PD takes place by means of an InP membrane input waveguide. The detector is stacked on top of that and the optical power is detected in the absorption layer. The membrane coupler (right) was studied with a 3D modal analysis, considering the three sections shown in the figure.

schematically in Fig. 1. The PD structure is built as a 700 nm InGaAs absorption layer sandwiched between a highly p-doped InGaAs contact layer and a highly n-doped InP layer, which is also used for realizing the membrane waveguide.

The coupling between the InP and the Si waveguides was studied performing a 3D modal analysis. First, the mode indices of the fundamental mode propagating in the Si and InP waveguides and of the even and odd system modes excited in the coupling structure were calculated. Then, the excitation coefficients were calculated by overlapping the Si waveguide fundamental mode and the even/odd system mode. The system modes propagate along the coupling region with different propagation constants $\beta_{even/odd}$, and after a distance $L_c = \frac{\pi}{\Delta\beta}$, defined as coupling length, the maximum transfer of optical power occurs from the Si to the InP waveguide. The difference $\beta_{even} - \beta_{odd}$ is responsable for the system dynamics: by varying the waveguide geometry, different system modes are supported, with different propagation constants. Thus, the mode beating changes and, accordingly, the coupling length. As a last step, the coupling efficiency η_c was calculated by overlapping the fundamental mode guided by the InP waveguide with the field at the section $z = L_c$ (see Fig. 1, right). The calculations were done with the Finite Difference (FD) and the Film Mode Matching (FMM) calculation methods implemented in two different full vectorial mode solvers: Selene, by C2V, and FIMMWAVE, by Photon Design, respectively. Fig 2 (left) shows the mode indices for the coupled waveguides calculated with those two methods. By properly choosing the InP waveguide dimensions, mode matching can be achieved with the Si waveguide, which is 500 nm wide and 220 nm thick. We fixed the InP waveguide thickness to 250 nm, which leads to a predicted optimum waveguide width of 1 μm (0.8 μm), calculated with the FD (FMM) method. When choosing a thinner InP waveguide, e.g. 200 nm, simulations show that the mode matching does not occur. On the other hand, going for a larger thickness would lead to a narrower waveguide, which is more difficult to fabricate. According to the simulations, the predicted coupling length varies between 12 and 14 μm, depending on the calculation method used, and a power coupling efficiency of more than 80% can be achieved with a tolerance of $\pm$100 nm for the InP waveguide width (see Fig. 2, right), which is well within the current technology limitations. The PD structure shown in Fig. 1 allows the fabrication of laterally tapered membrane waveguides without additional processing steps, which provides an increase of the alignment tolerance between the waveguides. The device fabrication is described

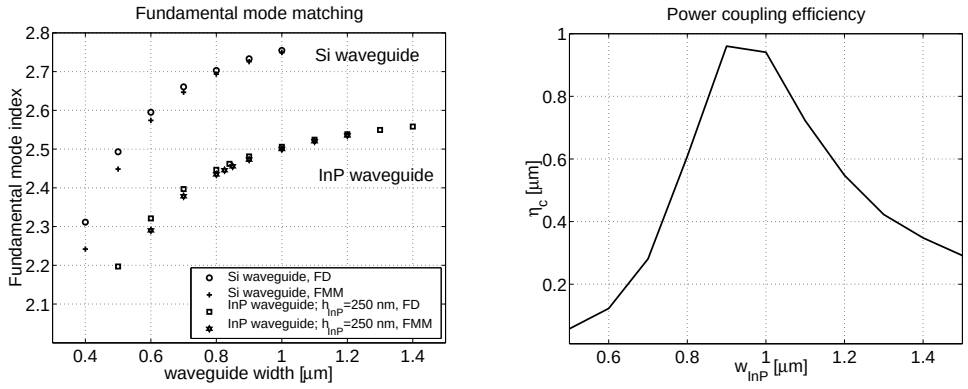

Figure 2: Left: Mode index. Right: Coupling efficiency as a function of the InP waveguide width. The thickness of the membrane waveguide is 250 nm. In this configuration, a power coupling efficiency of more than 80% can be achieved with a tolerance for the InP waveguide width of ± 100 nm.

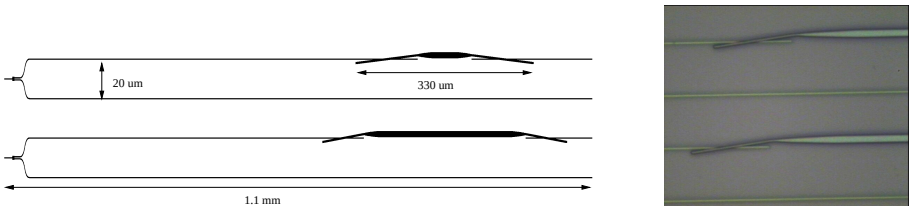

Figure 3: Left: a zoom of the coupler mask layout is shown, overlapped with the Si waveguide pattern. The Si waveguides are split into the upper test branch, over which the InP couplers were fabricated, and the lower reference arm. Slanted coupler layouts are shown in this figure. Right: photograph of the fabricated slanted membrane couplers taken with optical microscope.

in the next section.

Coupler fabrication

Several types of couplers were designed, including straight, laterally tapered, and slanted waveguides. Moreover, couplers with different width, length and lateral offset with respect to the Si waveguides were designed to compensate possible fabrication errors and simulation discrepancies. For the ease of the measurements, the Si waveguides are split into two branches, one of which is used as a reference arm, as can be seen in Fig. 3, left.

The waveguide structure was epitaxially grown on a 2 inch InP substrate. The wafer was then bonded upside down on a SOI wafer, in which the Si wiring had been defined. A 300 nm SiO_2 layer had been deposited at the bonding interface in order to achieve molecular bonding. Afterwards, the InP wafer substrate was wet-chemically removed and the bonded wafer diced. The die processing started with a RIE step to open the alignment markers in the Si layer, underneath the bonded area. Those markers were then used to align the membrane waveguides over the Si wires. This was the most critical step, due to the small waveguide dimensions and the step height between the waveguide layers. After waveguide lithography, the couplers were fabricated by using a combination of wet and dry etching steps. The characterization of the devices is currently under way.

Processing of full PDs like the one shown schematically in Fig. 1 is also currently being done. Two InP-based 2 inch wafers with, respectively, PD and laser layer stacks

were grown and diced in 9×7 mm^2 pieces.

The dies were then bonded upside down on a SOI wafer, in which the Si waveguide pattern had been defined, and the die substrate was wet-chemically removed. Afterwards, samples containing both source and PD dies and test samples with only the source or the detector die were sawn. Sources and PDs patterns were defined by e-beam lithography and transferred to a 150 nm thick SiO_2 hard mask. The same hard mask was then used to dry-etch the membrane waveguides and the PD bottom contact areas, which share the same n-InP layer. The PD mesas were wet-chemically etched (see Fig. 4). We are currently working on the final passivation and metallization processing steps, after which the device characterization will start.

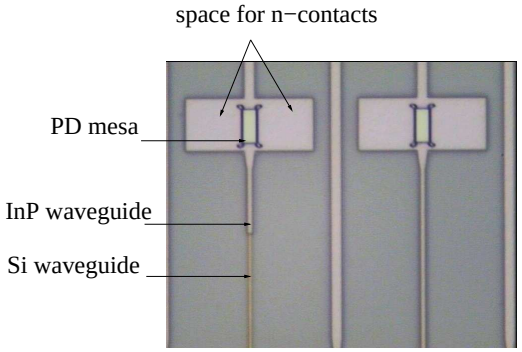

Figure 4: Two PDs are shown in this picture taken with optical microscope. The detector input InP waveguides are aligned over the Si wires and tapered out towards the absorption area underneath the mesas.

Conclusions and acknowledgement

We presented the design of a photodetector structure suitable for integration on an optical interconnect layer on top of CMOS ICs. The device uses an InP membrane input waveguide to couple the optical signal out of the interconnect layer. A 3D modal analysis was performed to design the membrane coupler and predict its performance. It is shown that a 250 nm thick by 14 μm long coupler has a predicted efficiency of more than 80% with a fabrication tolerance for the waveguide width of $1\,\mu\text{m} \pm 150\,\text{nm}$. We are currently working on the device characterization and the PD fabrication.

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References

[1] *International Technology Roadmap for Semiconductors (ITRS)*. http://public.itrs.net.

[2] C. Piguet, J. Gautier, C. Heer, I. O'Connor, and U. Schlichtmann, "Extremely low-power logic," in *Proc.of the Design, Automation and Test in Europe Conference and Exhibition (DATE'04)*, vol. 1, pp. 656–661, Feb. 16-20 2004.

[3] D. Van Thourhout, P. Dumon, W. Bogaerts, G. Roelkens, D. Taillaert, G. Priem, and R. Baets, "Recent progress in SOI nanophotonics waveguides," in *Proc. 31st Eur. Conf. on Opt. Comm. (ECOC '05)*, pp. 241–244, Glasgow, Scotland, Sep. 25–29 2005.

[4] D. Van Thourhout, G. Roelkens, J. Van Campenhout, J. Brouckaert, and R. Baets, "Technology for on-chip optical interconnects," in *LEOS Annual Meeting 2005*, Sydney, Australia, Oct. 2005.

[5] H. Hattori, C. Seassal, E. Touraille, P. Rojo-Romeo, X. Letartre, G. Hollinger, P. Viktorovitch, L. Di Cioccio, M. Zussy, L. E. Melhaoui, and J. Fedeli, "Heterogeneous integration of microdisk lasers on silicon strip waveguides for optical interconnects," *IEEE Photon. Technol. Lett.*, vol. 18, pp. 223–225, Jan. 2006.