InP-based membrane photodetector for optical interconnections on CMOS ICs

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We demonstrate a compact photodetector suitable for photonic interconnections on electronic ICs. In such applications, the InP-based optical sources and detectors are linked via Si photonic waveguides in an interconnection layer on top of the CMOS circuitry. The photonic device processing is compatible with Si wafer scale fabrication steps, which guarantees compatibility with future IC manufacturing. In our approach, an InP membrane waveguide is used to couple the light out of the interconnection layer and carry it towards the detector absorption region. A responsivity of 0.45 A/W and an electrical frequency response 3-dB cut-off point at 15 GHz were measured.

Introduction

For future generation Si ICs, a bottleneck is expected at the interconnect level. The integration of optical sources, waveguides and detectors forming a photonic interconnect layer on top of the CMOS circuitry is a promising solution, providing bandwidth increase, immunity to EM noise and reduction in power consumption [1, 2, 3]. This solution was investigated within the European project PICMOS[1]. In that context, the interconnect layer is built as a passive Si waveguide layer and the photonic sources and detectors are fabricated in a way compatible with wafer scale processing steps, assuring compatibility towards future generation electronic ICs. The integration technique investigated here combines the advantages of high quality Si wires with the excellent properties of InP-based lasers/detectors and is based on a die-to-wafer bonding technology [4]. Experimental results on a full optical link, including lasers and detectors, were reported in [5]. In this paper, we focus on the detector design, fabrication and characterization.

Design

The optical signal has to be coupled first from the Si wire into the detector structure to be absorbed. In our approach, that is realized by means of an InP membrane input waveguide on top of the SOI wafer containing the Si photonic wiring, like shown schematically in

[1]Photonic Interconnect Layer on CMOS by Wafer-Scale Integration (PICMOS), http://picmos.intec.ugent.be

Fig. 1. The two waveguides act as a synchronous coupler that couples the light from the Si wire into the transparent InP waveguide that guides it to the absorbing region on top of the transparent layer. The PD structure is built as an n.i.d. 700 nm InGaAs absorption layer sandwiched between a highly p-doped 50 nm InGaAs contact layer and a highly n-doped 250 nm InP layer, which is also used for realizing the membrane waveguide, and has a footprint of $5 \times 10\ \mu m^2$. We chose a device thickness of $1\ \mu$m in order to ease integration with the μ-disk lasers described in [6] and to optimize the trade-off between device speed and internal quantum efficiency, which were predicted to be 25 GHz and 70%, respectively. The input InP waveguide was designed 250 nm thick and $1\ \mu$m wide to achieve mode matching with the Si wire. For such a structure, simulations predict a coupling length of around $14\,\mu$m and a coupling efficiency of more than 80% with a tolerance of ± 150 nm for the InP waveguide width, which is well within the current technology limitations. For more details about the detector design, we refer to our previous work described in [7, 8].

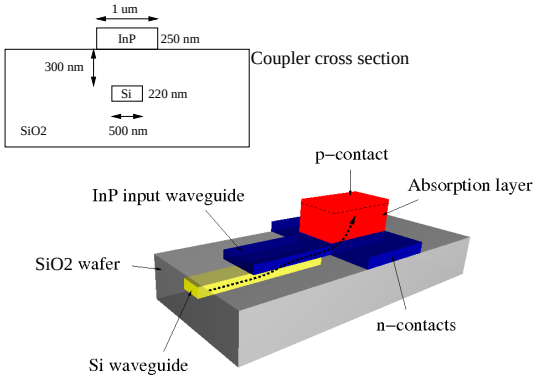

Figure 1: Photodetector structure. The coupling from the Si photonic waveguide layer to the PD is realized by means of the InP membrane input waveguide, on top of which the detector is stacked. A cross section of the coupler is schematically shown.

Fabrication

The PD layer stack was grown on a 2" InP wafer, which was sawn in dies that were then bonded upside down on an SOI wafer, in which the Si waveguide pattern had been defined. The bonding technique consists in depositing a 200 nm thick layer of SiO_2 on top of the Si waveguides and a 100 nm thick SiO_2 layer on top of the InP wafer. After polishing, the van der Waals molecular bonding forces at the SiO_2-to-SiO_2 interface provide die-to-wafer adhesion [4]. Then, the InP substrate was wet-chemically removed from the dies, the PD pattern was defined by e-beam lithography with precise alignment to the silicon waveguide and transferred to a 150 nm thick SiO_2 hard mask and the SOI wafer was sawn into samples hosting one photonic die each. Membrane waveguides, PD bottom contact areas and PD mesas were etched with a combination of dry- and wet-chemical ething steps. Then, a polyimide layer was deposited to planarize the chip surface and provide electrical isolation. Finally, top- and side-contact windows were dry-

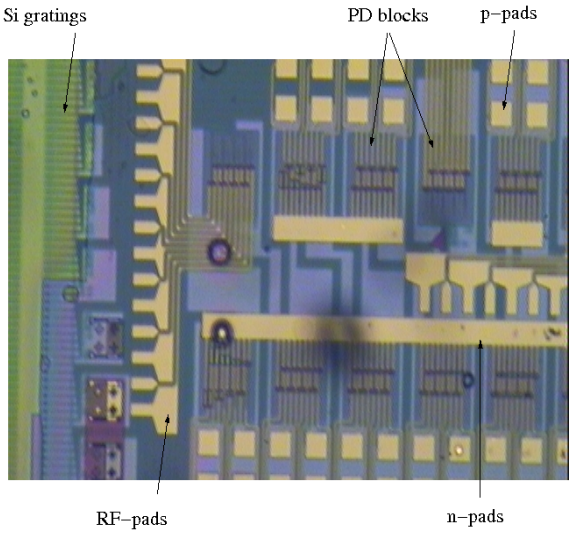

Figure 2: Picture of the fabricated chip. Ten PD blocks (8 devices/block) are shown.

etched and a Ti/Pt/Au metal layer stack was evaporated and patterned by lift-off. Fiber gratings, as described in [9], were also integrated in the Si waveguide layer to allow characterization of detectors without the need of a full optical link fabrication (see Fig. 2).

Measurement Results

The device characterization was performed by using a tunable laser source (TLS) and a polarization controller to couple TE-polarized light through the grating coupler into the Si waveguide. The photodiode generated photocurrent was measured with a Keithley source-meter unit, which was also used to reversely bias the PD. Dark currents around 1.6 nA were registered at -4 V. To evaluate the detector efficiency, the following loss

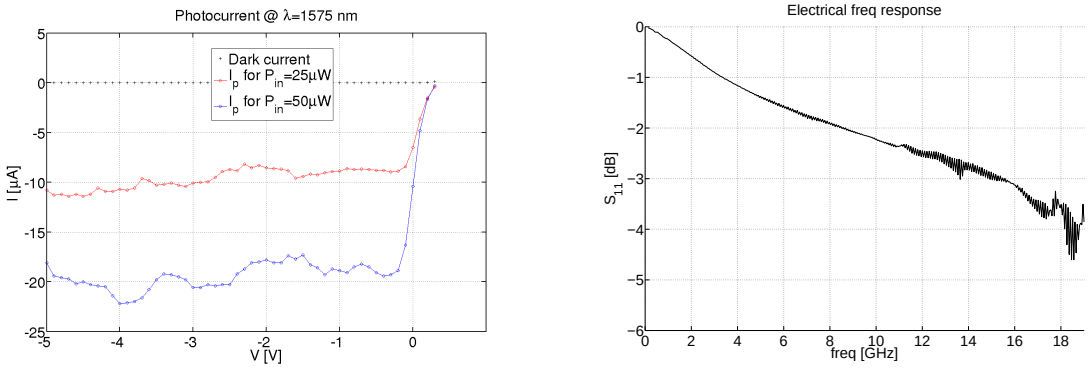

Figure 3: Left: Photocurrent for 0 μW, 25 μW and 50 μW optical input power as a function of the detector applied bias voltage. Right: Electrical frequency response of the detector structure.

factors were first measured: fiber connections from the TLS to the polarization controller (0.7 dB), Si grating coupling efficiency (max. 20% at $\lambda = 1575$ nm), Si waveguide propagation loss (4-5 dB/cm for TE). Taking those loss sources into account, the detector optical input powers corresponding to TLS intensities of 0 mW, 0.2 mW and 0.4 mW were estimated to be 0 μW, 25 μW and 50 μW, respectively (Fig. 3, left). Thus, a responsivity of $R = 0.45$ A/W was conservatively calculated, assuming the maximum grating coupling efficiency. Such responsivity corresponds to a quantum efficiency $\eta = 35\%$, which agrees quite well with predicted values, as it includes both the efficiency of the InP membrane coupler and the internal quantum efficiency of the pin-detector.
Dynamic characterization in the frequency domain was performed to investigate the electrical frequency response of the detector structure. A 20 GHz network analyzer was used for sending an RF electrical input signal to the PD and for receiving the reflected RF power. A 65 GHz bias-tee was used to separate DC and AC components and bias the detector, while an RF probe was used for contacting the RF pads on the chip. After measuring, we de-embedded the parasitic effects caused by the mismatch of the RF set-up components, namely high frequency cables, connectors, bias-tee and probe. This data-processing was performed by following standard methods reported in [10, 11, 12]. Fig. 3 (right) shows the S_{11} parameter after the de-embedding: the 3-dB cut-off point is at 15 GHz. The deviation with respect to the simulation results comes from the mismatch of the transmission line between the PDs and their RF pads (see Fig. 2), mainly due to the uncertainty in the polyimide electrical permittivity at RF frequencies. We are currently busy with the optical-to-electrical dynamic characterization.

Conclusions and Acknowledgment

We presented an InP-based photodetector fabricated on a bonded SOI wafer containing Si waveguides, suitable for an optical interconnect layer on top of CMOS ICs. The PD footprint is $5 \times 10\ \mu m^2$ and an InP membrane input waveguide is used to couple the optical signal out of the interconnect layer. Measurements recorded a detector responsivity R=0.45 A/W and an electrical frequency response 3-dB cut-off point at 15-GHz.
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