Reflectivity measurements of deeply etched DBR gratings in InP-based double heterostructures

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A three-level masking process has been developed for etching DBR gratings in InP/InGaAsP double hetero-structures. The masking consists of a ZEP/Cr/SiO_x layer stack. The ZEP layer is used to open the Cr which is a good mask for etching anisotropically the SiO_x layer. The InP-based double heterostructure is etched in an ICP process using Cl_2:Ar:H_2. With this process deep etched waveguides are simultaneously etched with the DBR gratings with various numbers of periods (1 to 5). 2 µm wide waveguides show a loss of 3 dB/cm and the reflectivity of a 2 period DBR grating was found to be 80%.

Introduction

Deep etched distributed Bragg reflector (DBR) gratings are very useful building blocks for InP/InGaAsP-based photonic integrated circuits (PICs). In theory, a first order deep etched grating can achieve a reflectivity of more than 97%, within only a few grating periods [1]. The small size and high reflectivity of the DBR gratings allows the fabrication of ultra small, in-plane lasers [2-3] that can be applied in photonic logical circuits.

The realization of these sub-micrometer scale structures is very challenging. Being able to integrate the DBR mirrors with other photonic components adds additional restrictions to the fabrication process. We present our first measurement results of deeply etched DBR gratings fabricated using electron beam lithography and inductively coupled plasma (ICP) etching, which is compatible with our conventional active-passive integration technology [4].

Grating design

For the deep etched DBR grating design, we took a double heterostructure consisting of an n-type InP substrate, 500 nm Q1.25 passive waveguide layer and 1.5 µm p-type InP top cladding as a starting point (see fig. 1). This layer stack is compatible with our standard active-passive integration platform, so the DBRs can be used in complex photonic integrated circuits.

Our aim is to get the highest reflectivity in the smallest number of grating periods, reducing the mirror loss to a minimum. To achieve this, a first-order grating design should be applied. This means that the width of the trenches etched into the semiconductor should be equal to ¼*λ/n, where λ is the central wavelength in vacuum and n is the refractive index of the material inside the trenches. After etching the

waveguide and DBR gratings this material is of course air, but one might want to fill the gratings later on by for example polyimide or BCB which are commonly used for planarization of optical chips. If some polymer is chosen as the filling material the reflection per period is lower than in the case of air. However, the out-of-plane diffraction is also lower, resulting in a better over-all performance. This is shown in figure 2. The gratings that were characterized in this work were filled with BCB (n≈1.5), resulting in a trench width of 258 nm.

The trenches are separated by thin semiconductor lines. The width of the lines of a first order grating is given by ¼*λ/N_{eff}, where N_{eff} is the effective refractive index of the mode in the waveguide. The mode profile was calculated for a 1.5 µm wide deep-etched waveguide, see figure 3. It is clearly visible that the mode field extends well below the Q1.25 waveguide layer. This means that to obtain the highest reflection, the trenches should be etched at least 1.5 µm into the substrate. For the calculated N_{eff} of 3.23 the width of the grating lines becomes 119 nm.

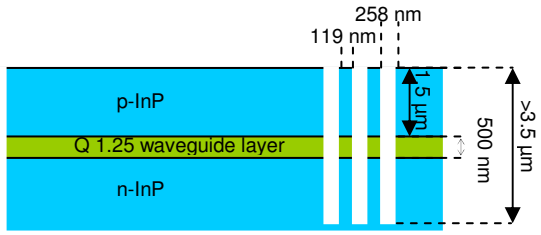

Figure 1: DBR grating design

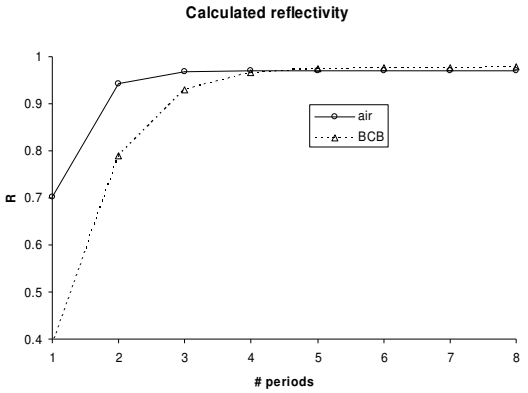

Figure 2: Calculated grating reflectivity for gratings in air (solid line) and BCB (dashed line)

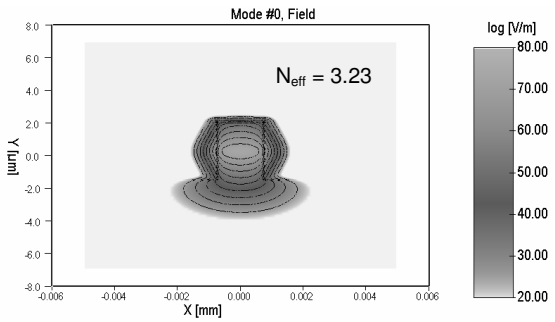

Figure 3: Logarithmic presentation of the field in a 3.5 µm deep etched waveguide

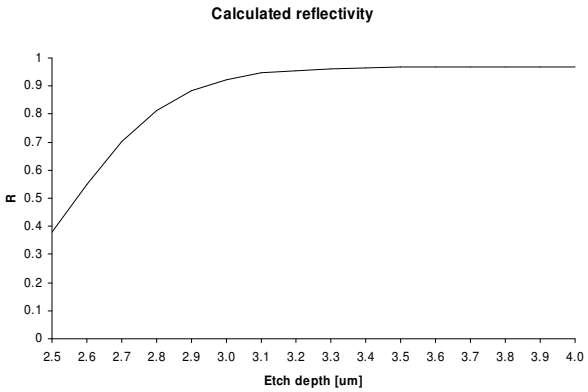

Figure 4: Calculated reflectivity of a 3-period DBR grating in air

Fabrication process

For the fabrication of the DBR chip a two step lithography process was used, as shown in figure 5. First, a 440 nm thick SiO_x layer was deposited by PECVD. Next a 50 nm thick chromium layer was deposited by e-beam evaporation. Finally a ZEP e-beam

resist layer of 320 nm was applied in which the grating pattern was written. The width of the lines is 20 nm less than the trench widths calculated previously. This is done to compensate for forward scattering during the e-beam exposure. The lines are 10 µm long. This allows easy alignment with the waveguides later on, but also avoids problems due to the proximity effect in the 30 kV e-beam exposure, which is more profound at the end of the lines.
After the e-beam exposure using a Raith-150 machine, the pattern is transferred into the chromium layer by Cl_2:O_2 inductively coupled plasma (ICP) etching, using low RF powers [5]. Next the e-beam resist is removed with a chemical stripper and then an optical photoresist layer (HPR504) is spun on the patterned chromium. Several waveguides with widths between 1.0 and 4.0 µm are defined by optical lithography and are also transferred into the chromium with the same ICP process. The photoresist is removed chemically and then the chromium layer serves as a mask in a CHF_3-based RIE process to transfer the pattern into the thick SiO_x layer.
Finally the pattern is etched into the InP/InGaAsP/InP layer stack with an ICP etching process using a Cl_2:Ar:H_2 chemistry. The ICP process gives us high plasma densities, resulting in high etch rates (~2 µm/min), but operates at lower DC bias voltages, compared to conventional RIE processes. This results in less etching damage to the lattice and therefore very smooth sidewalls. The thick SiO_x mask allows us to etch sufficiently deep, also inside the grating trenches.

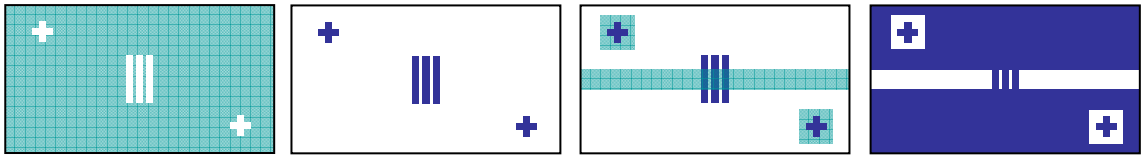

Figure 5: Lithography process. First, the DBRs are written by e-beam lithography (a), then the DBR pattern is etched into the chromium mask (b), then the waveguides are defined by optical lithography (c), and are also etched into the chromium mask (d).

Reflectivity measurements

To determine the reflection properties, a Fabry-Perot based method was applied. First, the propagation losses as a function of waveguide width were determined using some waveguides without DBR gratings and cleaved facets. Looking at the transmission spectrum, the propagation losses can be determined from the fringe pattern, using calculated values for the cleaved facet reflectivity. The results are shown in figure 6.
Then one of the facets was coated with an anti-reflection coating. The waveguides that contained the DBRs formed another Fabry-Perot cavity, but now between one cleaved facet and one DBR grating. Knowing the propagation losses from the first measurements, the DBR reflectivity could be calculated.
The measured reflectivities are shown in figure 7. In the graph, 1 grating pair corresponds to 1 trench in the waveguide (generating 2 reflections, one at the semiconductor-air interface and one at the air-semiconductor interface). 2 grating pairs are 2 trenches, etc.
For 1 and 2 grating pairs the measured reflection matches the values predicted by simulation. For 3 pairs and higher, the spread in measured points is much larger. The average value of the reflection seems to saturate around 80%. This could be due to the

small transmission signal that is measured, resulting in a larger signal-to-noise ratio, which also explains the larger spread in measured values. Another explanation could be that at a larger number of grating pairs, the phase relation becomes more stringent. This means that the grating performance is less tolerant to fabrication imperfections. However, simulations show that the grating dimensions must deviate more than 80 nm in order to explain the lower reflectivity by this effect only. After inspection of the gratings from the top using a SEM this seems unlikely.
The final possibility is that the etch depth inside the gratings is lower than expected. This is difficult to determine accurately, since it requires cleaving exactly through one of the gratings.

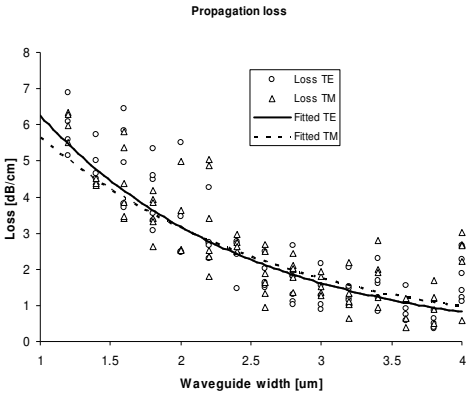

Figure 6: Measured propagation losses

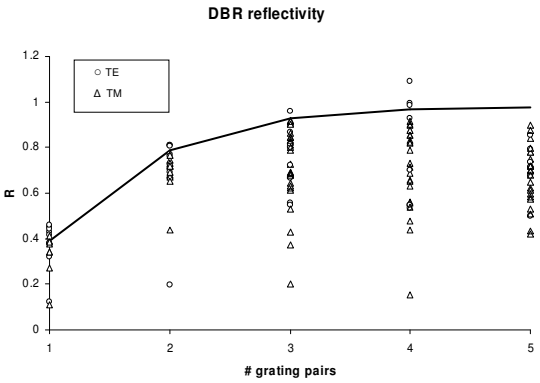

Figure 7: Measured DBR reflectivity

Conclusion

We developed a simple and robust fabrication technology for the fabrication of deep-etched DBR gratings. We have fabricated low loss deep etched waveguides, with DBR gratings that show reflections up to 80%. For 1 and 2 DBR periods the measured reflections match the calculated values, but for higher number of periods the reflection seems to saturate and the spread in measured values increases.

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