Photonic integrated circuits for data read-out systems

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We propose and design two photonic integrated circuits which can be used in a data read-out system. The designs are developed for use in a neutrino detector but the principle is applicable to a wider range of read-out systems. The first one is an optical serializer integrated with electro-optical modulators and semiconductor optical amplifiers and operates at a single wavelength. The second one employs a wavelength-division-multiplexing scheme and utilizes arrayed waveguide gratings, electro-optical modulators and semiconductor optical amplifiers.

Introduction

Time division multiplexing plays a key role in modern optical communication systems. It enables to increase the capacity of data transmitted in a single fibre link. Electronic multiplexers can now reach a speed of 165 Gb/s [1]. However, multiplexing of signals in optical domain can reduce power consumption and increase the output bit-rate. Latest experiments showed that transmission of 1.28 Tb/s signal is possible [2].

Serialization of multiple input optical signals can be done by using various methods. The first one is application of delay lines [3]. The signals in parallel channels appear at the output at strictly dedicated time slots due to a different propagation length in each of the signal paths. Other techniques utilize wavelength conversion phenomena such as four wave mixing [4], differential frequency generation [5] and cross-phase modulation [6]. In these systems parallel input signals (λ_s) are used to modulate an optical carrier (λ_c). As a result a modulated output signal at wavelength λ_c [6], or $2\lambda_c - \lambda_s$ [4, 5] is generated. Wavelength conversion takes place in a semiconductor laser amplifier [4], periodically poled lithium niobate [5] or highly non-linear fibre [6]. However, these techniques also require appropriate time adjustment, provided by the previously mentioned delay lines. Cross-phase modulation is also used in multiplexers that employ non-linear loop mirrors [7].

In this paper we will study the method utilizing delay lines in the framework of a neutrino detector read-out system.

Recent large scale physics experiments generate huge amounts of data, which has to be read-out and transmitted from the detector to the analysis station. An example of such an experiment is the European KM3NeT project, which aims to detect neutrinos from distant astrophysical sources. The data read-out unit for this telescope is one of ten pilot applications that are explored in the EuroPIC project. The main objective of EuroPIC is to develop the supply chain of a generic integration technology in photonics as it was done for CMOS.

In this work we propose two novel concepts utilizing photonic integrated circuits as read-out modules for KM3NeT. The first one is an optical serializer, where we multiplex, fully optically in the time domain, 32 electrical input signals. The second concept makes use of WDM technique and transmits these signals parallel.

System overview and fabrication technology

KM3NeT is a neutrino detector with a volume of a cubic kilometer, that is going to be built at the bottom of the Mediterranean Sea. The detector uses 192 000 photomultipliers to detect Čerenkov radiation originating from interaction of neutrinos with the sea water.

The basic component of the detector is an optical module (glass sphere) with 32 photomultipliers inside. They produce an analogue signal which is digitized using a time-over-threshold method. The data from each of the photomultipliers should be read-out with a sampling frequency of 1 GHz and transmitted from the underwater detector to the central station situated on shore, about 100 km from the detector. We are investigating the use of photonic circuits as an energy-efficient option to realize such a read-out system. The bit-error rate should be lower than 10^{-9} and the power dissipated inside each 32-channel circuit should be kept below 2.5 W.

EuroPIC makes use of an indium-phosphide (InP) technology platform that allows for monolithic integration of active and passive photonic components in a standardized technology. The circuit uses waveguides that are deeply etched with multi-quantum wells in the core layer for an increased electro-optical effect that makes use of the quantum-confined Stark effect. For a 1 mm long modulator the driving voltage for π phase shift is $V_\pi = 3$ V. Low-loss transitions between active and passive regions are available.

Optical serializer

The readout system makes use of a fibre link between the central station on the shore (transmitter and receiver) and the optical module (modulator) in the sea. An optical carrier, Gaussian pulses with a duration of 30 ps and 1 GHz repetition rate at $\lambda = 1.55$ µm, is sent from the shore to the photonic chip where it is split, modulated by the 32 photomultiplier output signals, serialized and reflected. The signal is detected in the central station. Serialization of the signals enables operation at a single wavelength inside the photonic chip and to multiplex signals coming from various optical modules in the frequency domain.

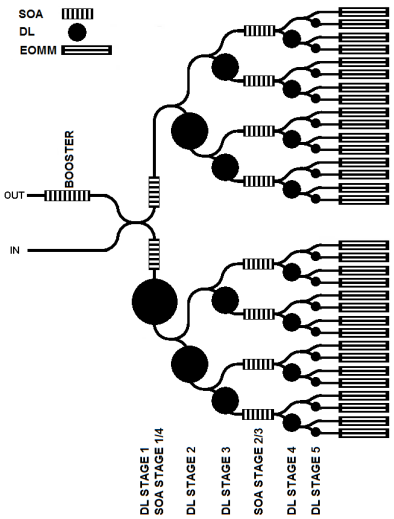

Fig. 1 Schematic of the optical serializer

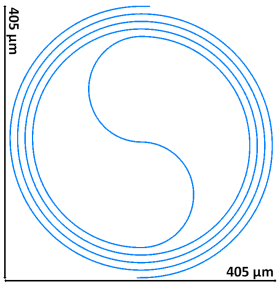

Fig. 2 Example of a spiral optical delay line L = 5 mm

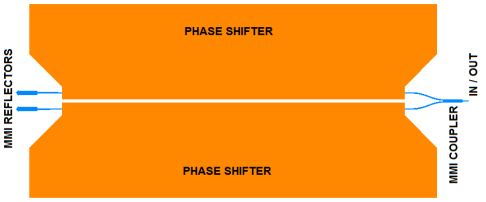

Fig. 3 Layout of the electro-optical Michelson modulator

A schematic of the integrated optical serializer is shown in Figure 1. It operates in reflecting configuration, which helps to reduce the size of the circuit and the number of

components used. The optical carrier appearing at the input is split among 32 waveguides by five stages of 3-dB multi-mode interference couplers. Simultaneously it is gradually delayed by optical delay lines (DLs) and amplified by semiconductor optical amplifiers (SOAs). At the end it is modulated by electro-optical Michelson modulators and sent back through the same splitting network which now acts as a combining network. Finally, before the output the signal is amplified by a booster amplifier. Details of the design are described below.

Serialization -- Serialization is provided by optical delay lines. An example of a DL is presented in Figure 2. It is a waveguide folded into a spiral. The footprint of a DL is determined by the minimum bending radius.

A staged distribution network is applied to reduce the total length of the delay lines. Instead of using 31 delays after a 32-fold split, we apply one delay after each MMI splitter. The length of the DL is twice as small as in the preceding stage. The shortest incremental delay is $\Delta\tau_{ch}$ = 31.25 ps (1/32 ns), which requires a length of 1269.45 μm corresponding to $\Delta\tau_{ch}/2$ as the light passes through it twice.

Modulation -- The chip has to read-out the data from the photomultipliers. As the serializer operates in a reflecting configuration, an electro-optical Michelson modulator has been applied (Figure 3). When light enters the modulator, it is split by 1:2 MMI coupler. After propagation through the phase-shifting section it is reflected by an MMI reflector. In absence of the modulation voltage, the light interferes constructively at the output of the MMI coupler. However, when the appropriate voltage in one of the branches is applied, the phase-shift causes destructive interference and there is no signal at the output.

Power compensation -- There are two sources of losses in the circuit. The first one is due to the 32-fold power splitting. The other is due to the propagation and insertion losses of the optical components. Semiconductor optical amplifiers are used to compensate these losses. The gain of each amplifier is set differently, to compensate the different attenuation that each signal experiences. The maximum power imbalance among the channels is ΔP = 1.2 dB.

WDM circuits

An alternative to the system employing the serializer circuit is a parallel read-out of the photomultiplier data. Two wavelength-division-multiplexed (WDM) photonic integrated circuits are used as read-out units. The system utilizes 32 wavelengths with each a bit-rate of 1 Gb/s. Schematics of the two circuits are shown in Figures 4 and 5.

The first circuit is designed in a reflecting configuration. The input signals, 1 GHz

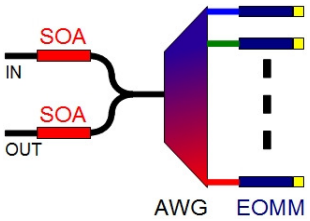

Fig. 4 WDM circuit in reflecting configuration

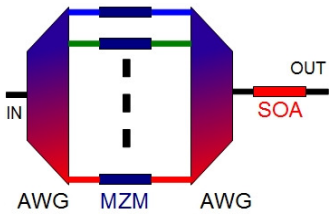

Fig. 5 WDM circuit in transmitting configuration

optical pulse-trains, are demultiplexed by an arrayed waveguide grating (AWG) and each channel is modulated by the electro-optical Michelson modulator described in the previous section. After reflection the same AWG multiplexes all of the channels. The second circuit makes use of two AWGs – the first one demultiplexes input signals among 32 waveguides, then they are modulated in Mach-Zehnder modulators, and

separate AWG is used to multiplex them again. In both circuits semiconductor optical amplifiers are used to compensate the losses introduced by the circuit components.
Better performance may be expected from the transmitting circuit as the attenuation is higher in the reflecting configuration, due to the extra MMI and reflectors. However, the passbands of the two different AWGs might be misaligned, causing additional loss. Furthermore, the footprint is twice as large, compared to the reflecting configuration.

Mask layout

Figure 6 presents a mask layout of the test circuits measuring 6 mm x 6 mm in total. Since in this first realization the devices are meant as proof-of-concept, the circuits were simplified to have eight channels each. Two variants of each circuit are shown in the figure.

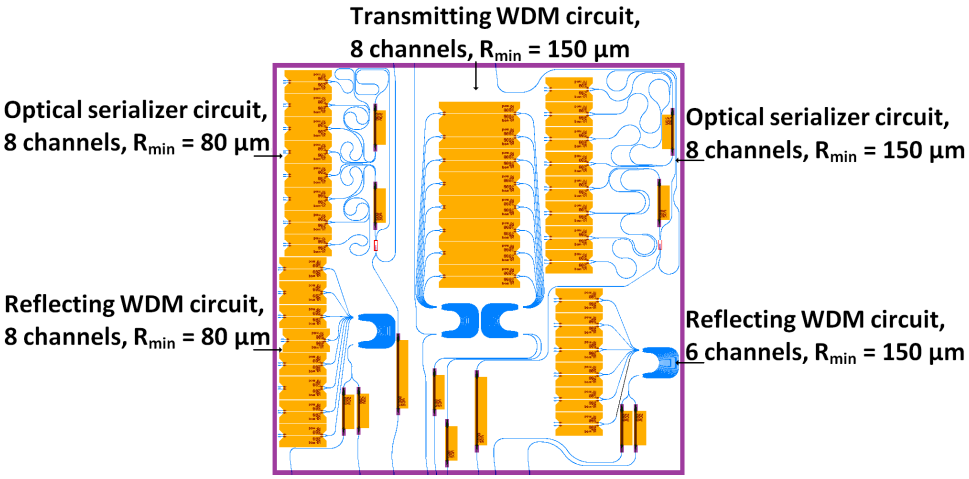

Fig. 6 Mask layout of the test circuits

Summary and conclusions

We have presented two solutions for a data read-out system, to be tested in the framework fo the KM3NeT neutrino telescope. The mask layout has been designed in the process of an InP foundry.
The optical serializer is a novel concept that integrates optical delay lines, modulators and amplifiers. It performs both modulation and serialization on a single chip and has a potential for application in data read-out and transmission systems.
We acknowledge the support of the EU through the FP7 NMP project EuroPIC, CP-TP 228839-2.

References

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