System Demonstration of a InP WDM Optical Switching Module with FPGA-based Controller as Basic Block for Scalable OPS nodes

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We demonstrate the functionality of an FPGA controlled 4x4 InP monolithically integrated WDM cross-connect (WDM-OXC) followed by wavelength converters. We provide evidences that the WDM-OXC can be employed as basic block for building a large port-count optical packet switch with highly distributed control and low switching latencies. The switch control is based on an FPGA board that decodes the packet labels, solves possible output packet contentions and properly drives the WDM-OXC. We show error free switching operation of four 40 Gb/s NRZ WDM channels with 4 dB penalty. The overall module switching time is around 25 ns.

Introduction

The increasing demand of bandwidth-hungry emerging services like cloud-computing, social networking and video sharing, is rapidly boosting internet traffic growth [1]. As a consequence, data centers (DCs) have to handle large volumes of packetized data. Although optical links are already employed in these systems, the switching is performed by electronic packet switches. This translates in unavoidable optical-electrical-optical (O-E-O) conversions that effect the DC performance in terms of power consumption and end-to-end latency [2]. In this scenario, scalable optical packet switch (OPS) nodes may represent a valuable solution. In [3] a qualitative categorization and comparison of OPS architectures for DCs is reported. However, an OPS that scale to a large number of ports (>1000), while providing low latency does not exist yet. In this paper we experimentally investigate the feasibility of a scalable WDM OPS node architecture employing an FPGA-controlled integrated WDM-OXC module as basic building block.

WDM OPS architecture with distributed control

The OPS architecture experimentally investigated in this paper is shown in Fig. 1 (a). It is a strictly non-blocking architecture with N WDM input/output ports each of them carrying M WDM channels. The illustrated OPS architecture has a modular structure that allows for highly distributed control and nanosecond-scale switching times. Each WDM input is fed into an independent 1xN optical switching module (OSM). Each of the N OSMs handles M WDM channels and operates independently of the other OSMs. The N OSMs have one input and N outputs, each of them connected to a fixed wavelength converter (FWC). The FWCs solves the wavelength contentions between packets on the same WDM channels coming from different OSMs and destined to the same output port of the OPS. As shown in Fig. 1 (b), each OSM consists of a label extractor, a label processor, a 1xN WDM-OXC and a switch controller that drives the optical cross-connect according to the packets destinations. The 1xN WDM-OXC

consists of a broadcast stage (BS) and N parallel wavelength selective stages (WSSs), one for each module output. The WSSs consist of a 1xM array waveguide grating (AWG), M optical semiconductor optical amplifier (SOA) gates and a Mx1 combiner. Each OSM operates as follows. The in-band labelling and the parallel label processing techniques presented in [4] are employed in this work. The label extractor separates the labels and the payloads. The packet labels are optical-electrical converted and sent to the label processor. The packet payloads are fed into the WDM-OXC input remaining in the optical domain.. The switch controller reads the labels and drives accordingly the N WSSs of the WDM-OXC. It may happen that multiple packets on different WDM channels are destined to the same module output. In this case, the switch controller decides which packet is forwarded to the output according to a priority schedule. The controller enables only one of the SOA-based gates of each WSSs in order to connect only one of the M WDM channels to the module output. The selected packet is then fed into the FWC.

The modular structure of the described OPS architecture leads to two main advantages. Firstly, the time to configure the entire switching matrix is reduced to the time to configure a single OSM. Secondly, the performance of the entire architecture can be evaluated by studying the operations of a single OSM.

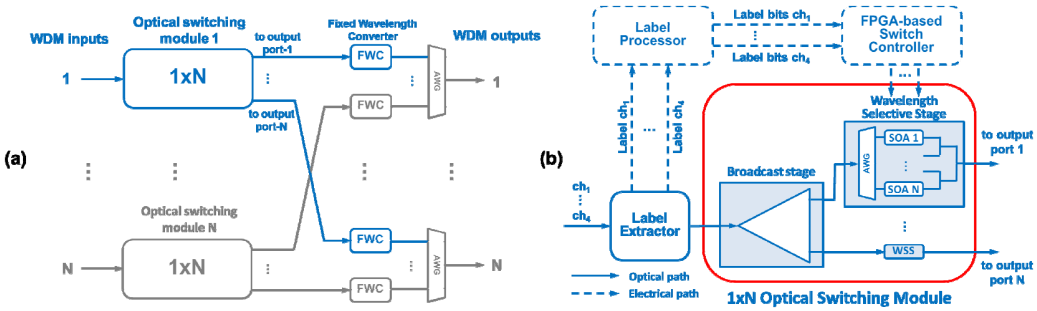

Fig. 1: WDM modular OPS architecture (a) and optical switching module implementation (b)

Experiment set-up and operation

Fig. 2 (a) shows the experimental set-up employed in this work. We consider a time slotted system. Four WDM lasers are modulated by an optical modulator driven by a pattern generator in order to obtain 4x40 Gb/s NRZ-OOK WDM packets with a duration of 290 ns and a guard band of 40 ns. The packet labels, synchronous with the payloads, are generated by an arbitrary waveform generator according to the RF tones labelling technique implemented in [4]. The employed WDM-OXC [5] is shown in Fig. 2 (b). It is a InP monolithically integrated 4x4 cross-connect. However, only one input of the device is used during this experiment to demonstrate the 1x4 OSM functionality. The integrated device consists of a BS and four parallel WSSs. The BS is based on cascade 1x2 MMI passive splitters. At each of the 4 outputs of the BS a 750 μm long SOA is used to compensate the splitting losses. Each WSS consists of a 1x4 AWG, four 140 μm long SOA gates and cascaded 2x1 MMI passive combiners. The labels are transmitted in the electrical domain to the label processor. Each label consists of two binary encoded RF-tones in order to address the four output ports of the OSM, as shown in Table I. The label processor detects the label bits of the four WDM packets in parallel and sends them to the FPGA-based switch controller. Synchronously, the packets payloads are optically transmitted to the WDM-OXC. The FPGA-based switch

controller decodes the label bits, solves output contentions and accordingly drives the SOA-based gates in the WSSs of the WDM-OXC.

Table I: output port-label bits map

	bit 1	bit 2
out 1	0	0
out 2	0	1
out 3	1	0
out 4	1	1

Table II: packets destinations as function of the time slot

	destination port per time slot									
ch1	3	1	4	4	3	2	1	4	1	2
ch2	2	3	2	1	4	3	2	2	3	1
ch3	**2**	4	3	**4**	**3**	**3**	**1**	1	4	3
ch4	4	2	1	3	**3**	**3**	3	3	**4**	4

The selected packets are then wavelength converted at the output of the OSM. The 40 Gb/s NRZ-OOK wavelength converter is based on non-linear polarization rotation in SOA [6]. At the output of the FWC the packets are detected and evaluated by a bit-error-rate (BER) analyser.

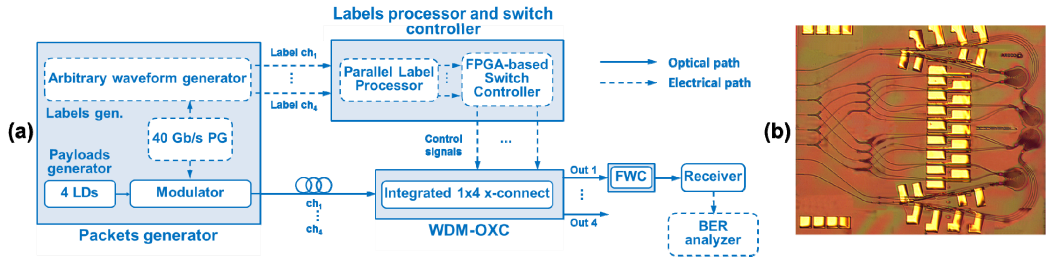

Fig. 2: experimental set-up (a) and photograph of the 4x4 integrated optical cross-connect (b).

Results

Four WDM packets (ch1=1548.1 nm, ch2=1551.2 nm, ch3=1554.5 nm and ch4=1557.7 nm) with an input power of 6 dBm/ch are coupled into the chip by using a commercially available lensed fiber array. We studied a periodic sequence of 10 time slots in which the packets are addressed as shown in Table II. The FPGA-based switch controller performs the contention resolution functionality according to a fixed priority scheme. Packets on ch1 have the highest priority, then packets on ch2 and so on. Packets that lose contentions are highlighted in Table II. Fig. 3 (a) shows the recovered label bits. We highlighted the packets destined to output three in order to verify the operation of the contention resolution functionality. Fig 3 (b) shows the control signals generated by the switch controller for the WSS 3 of the WDM-OXC. It is visible that in the fifth time slot packets on ch1, ch2 and ch3 are destined to output port 3 of the OSM. In this case the switch controller enables only the SOA-based gate associated with ch1. The control signals output from the digital pins of the FPGA board and are used to directly drive the SOAs in the WSSs. Each digital pin provides around 10 mA current, which is sufficient to enable the optical gates. Fig. 3 (c-f) show the switched packets at the 4 WDM-OXC outputs. BER curves in back-to-back, after switching and after wavelength conversion are shown in Fig. 3 (g). Error-free operation is achieved with 1 dB and 4 dB penalty after switching and after wavelength conversion, respectively. The overall switching time of the OSM is around 25 ns. Around 15 ns are needed to detect the label bits by the label processor, while 1 FPGA clock-cycle (10 ns) is sufficient to decode the packet addresses, to solve the contentions and to drive the WSS SOAs of the WDM-OXC.

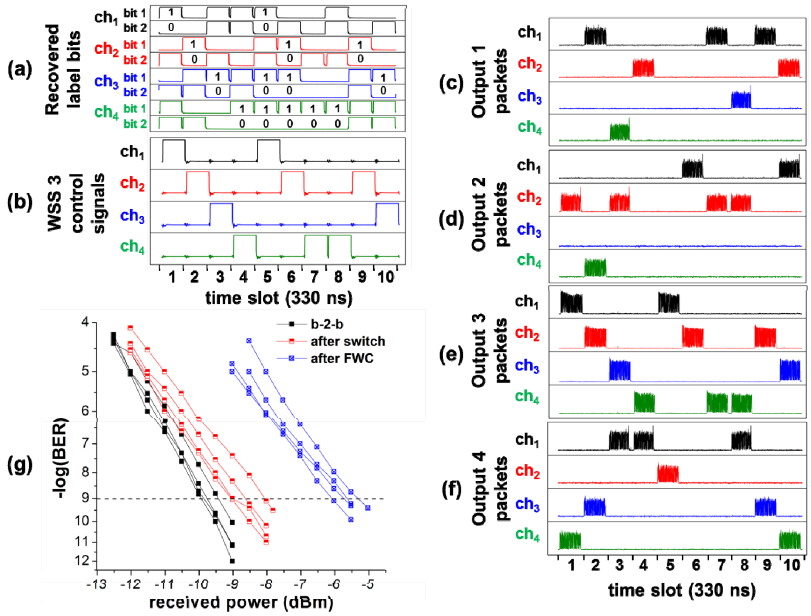

Fig. 3: recovered label bits (a), control signals for WSS 3 (b), output packets time traces (c-f) and BER curves in back-to-back (b-2-b), after switching and after fixed wavelength conversion (g).

Conclusions

We demonstrate the functionality of a 1x4 integrated WDM-OXC module and thus the feasibility of a 16x16 OPS based on the described architecture employing this module. The employed labelling technique and the parallel label processor in combination with the modular structure of this OPS architecture allow for nanosecond switching times. Scaling the WDM-OXC to 32 output ports will allow, considering 32 WDM channels per input, 1024 logical interconnections. While the parallel label processing makes the switching time port-count independent, realizing a 1024x1024 OPS (32 inputs carrying 32 WDM channels) is still challenging. It will require 32 1x32 WDM-OXCs with a 1x32 BS with 15 dB splitting losses, 32-channel AWGs with low loss and cross-talk operation, 1024 SOAs integrated on chip and FWC with broadband operation. Improvements in photonic integrating technology may allow the fabrication of such large scale photonic chip.

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