New Fabrication Method of Trapezoidal Polarization Converters

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We developed a new fabrication method of trapezoidal polarization converters whose sloping sidewalls are made by wet etching. The method consists in defining a mask for the top width of the converter, wet etching on both sides of the mask, protection of one sloping sidewall with resist, and dry etching the other sloping sidewall. In this way, critical dimension loss due to the wet etching becomes very small. First results show high efficiency of polarization conversion.

Introduction

There is a constant urge to reduce the sizes of optical components and increase the rates of data transfer. Photonic integrated circuits allow the transition from discrete optical components to integrated ones; so the sizes decrease very much. To increase the data transfer rates, different modulation schemes are used, for example, binary and quadrature phase-shift keying. There is a way to increase the transfer rates even more.

If we create two optical paths for light, we can modulate the signals separately. If we then put a polarization converter into one of the paths, after the paths recombine, we can analyze signals of orthogonal states of polarization separately and, in this way, double the transfer rate.

The usual fabrication of the polarization converter for InGaAsP-InP photonic integrated circuits has six critical steps and introduces an underetch [1, 2] which makes the efficiency of polarization conversion unreproducible. This paper suggests new fabrication of the polarization converter for InGaAsP-InP photonic integrated circuits. It has four critical steps and almost no underetch.

Description of polarization converter

Figure 1 shows the cross section and top view of the polarization converter. The layer stack of the converter has two layers: InGaAsP(1.06 μm) waveguiding layer and InP substrate. The input-output waveguides are 2-μm-wide and deep-etched. The converter has a trapezoidal cross section: the straight wall is made by dry etching and the sloping wall, by wet etching. The width of the input-output waveguides is 1.69 μm; the top width of the converter, 1.24 μm, the length of the converter, 275 μm. The critical parameter of the converter fabrication is the top width: its should not deviate by more than 50 nm from the designed top width because larger deviations give the efficiency of polarization conversion lower than 95 %.

The usual fabrication of the converter has six critical steps. Figure 2a shows the simplified processing: (1) lithography and dry etching to make a mask defining the converter top width; (2) lithography to cover one side of the mask to etch the straight wall of the

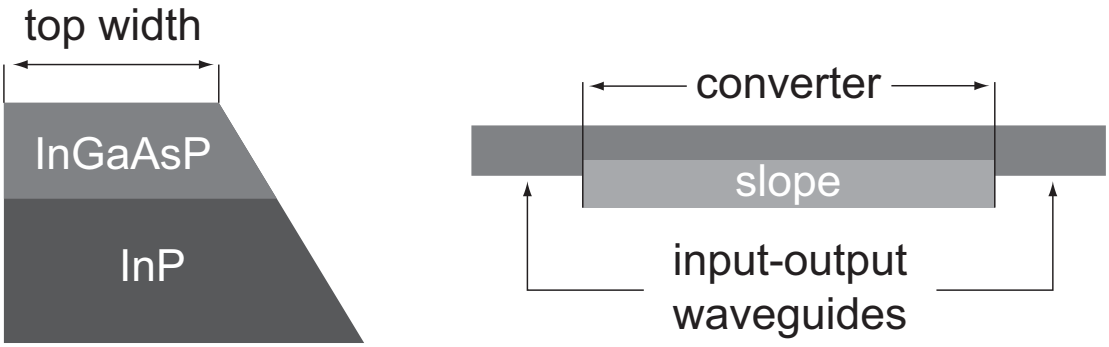

Figure 1: Schematic cross section and top view of trapezoidal polarization converter for InGaAsP-InP photonic integrated circuits.

converter; (3) dry etching to make the straight wall of the converter; (4) removal of the resist and deposition of the masking layer to protect the straight wall from the following wet etching; (5) dry etching of the mask to open flat surfaces for the wet etching; (6) the wet etching to make the sloping wall. The problem of this processing is in the sixth step. The mask layer covering the straight wall of the converter creates strain (Fig. 2a, step 6). The strain leads to a lift of the mask at the right edge and allows the wet etchant to go under the mask [1]. This lift gives an underetch of around 100 nm which is far beyond the 50-nm deviation. It is unacceptable for the reliable fabrication. To avoid the underetch, we need to have symmetric covering of the mask.

New fabrication of polarization converter

The new processing creates symmetric covering of the mask and has only four critical steps. Figure 2b shows them in a simplified way. Step 1, making the mask defining the top of the converter. We used the ZEP resist for electron beam lithography. The normal thickness of ZEP (about 300 nm) is not enough to etch 600 nm of a SiN_x mask; so we deposited a 50-nm-thick layer of Cr above SiN_x because Cr is more resistant than ZEP to the etching of the SiN_x. We then spun ZEP, baked it for four minutes at a temperature ramp from 100 to 150 °C and two minutes at 200 °C, and did the electron beam lithography. Next we developed ZEP in n-amyl acetate and rinsed the sample in methyl isobutyl ketone, followed by Cl_2-O_2 ICP etching of Cr, water rinsing, and pure CHF_3 reactive ion etching of the SiN_x mask. Step 2 was Br_2-CH_3OH wet etching to make sloping walls on both sides of the converter. Step 3, an optical lithography, made a 3-μm-thick layer of the AZ4533 resist to protect one sloping wall during the following CH_4-H_2 inductively-coupled plasma (ICP) etching. Step 4 was the ICP etching and removal of the AZ4533 resist by oxygen plasma.

We need to test each step of the fabrication. After step 1 of the processing, we check steepness and roughness of the SiN_x mask; after step 2, the wet etching by Br_2-CH_3OH, roughness of the sloping wall and the underetch; step 3 and 4, the optical lithography and ICP etching, steepness of the straight wall and coverage of the sloping wall by the resist. Figure 3 shows the scanning electron microscopy (SEM) images of the cleaves through the converter. After etching of the SiN_x, the walls of the mask are steep and slightly rough (Fig. 3a). The wet etching produces smooth slope and no visible underetch (Figs 3b and

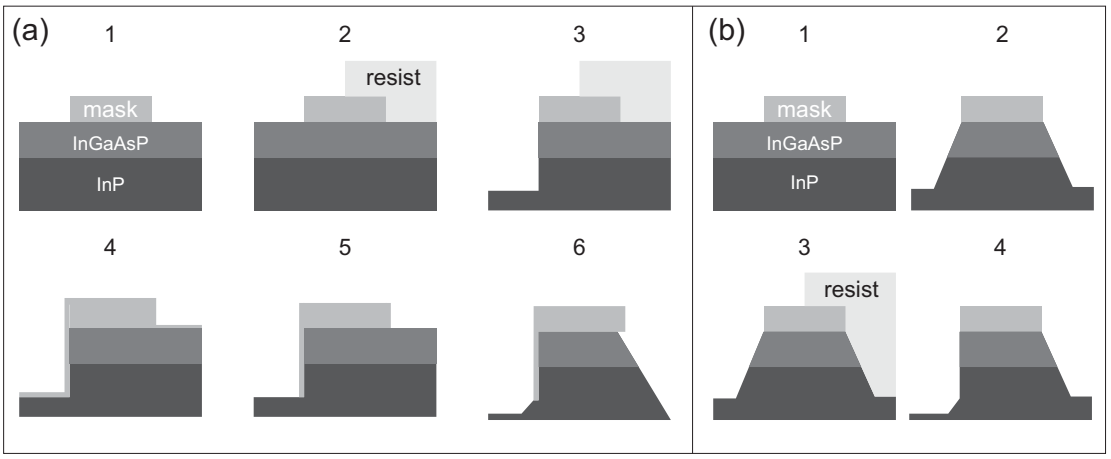

Figure 2: Simplified processing of polarization converter for InGaAsP-InP photonic integrated circuits. (a) usual processing: (1) lithography and dry etching to make masking layer that defines top width of converter; (2) lithography to cover one side of mask to etch straight wall of converter; (3) dry etching to make straight wall of converter; (4) removal of resist and deposition of masking layer to protect sloping wall of converter from following wet etching; (5) dry etching of mask to open flat areas for wet etching; (6) wet etching to make sloping wall of converter. (b) new processing: (1) lithography to make mask that defines top width of converter; (2) wet etching to make sloping wall of converter; (3) lithography to protect sloping wall of converter; (4) dry etching to make straight wall of converter and removal of resist.

3c). After the second lithography and the ICP etching, the straight wall of the converter is steep, the resist covers the sloping wall completely (Fig. 3c). Figure 3d shows the SEM image of the ready polarization converter.
We measured the efficiency of polarization converter and the loss of the converters. The efficiency was above 97 % and the loss, lower than 1 dB.

Conclusions

We suggested a new way of fabricating trapezoidal polarization converters for InGaAsP-InP photonic integrated circuits. This fabrication has only four critical steps in comparison with the usual processing. The steps are definition of the mask above the converter, Br_2-CH_3OH wet etching to make sloping walls on both sides of the converter, an optical lithography to protect one sloping wall, and dry etching of the second sloping wall to make the straight wall. The tests of these steps showed the following. The converter has a smooth sloping wall with no visible underetch; the sloping wall is not attacked during the dry etching of the straight wall. The straight wall of the converter is steep which is good for obtaining reproducible efficiency of polarization conversion. The preliminary measurements of the converters showed an efficiency of polarization conversion of more than 97 % and loss of less 1 dB.

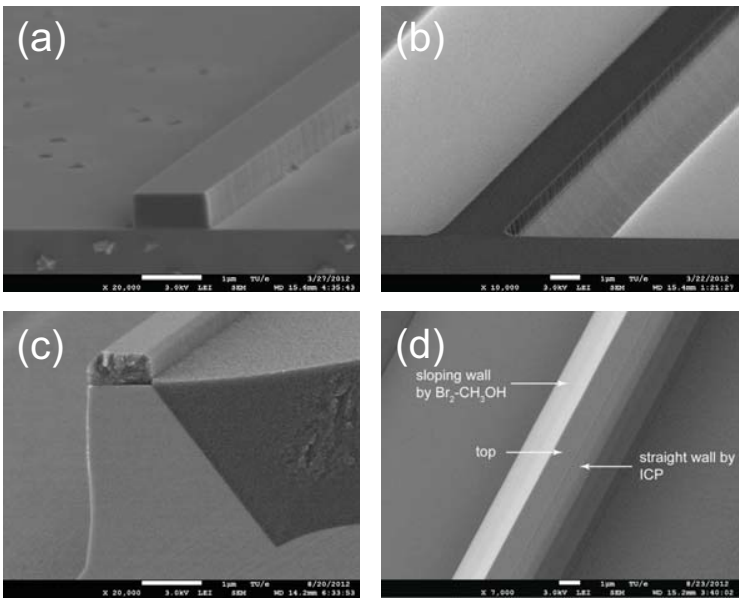

Figure 3: Images of scanning electron microscopy: (a) cross section through SiN_x mask; (b) tilted view on sloping wall of converter; (c) cross section through converter after inductively-coupled plasma etching; (d) top view on ready polarization converter.

Acknowledgments

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References

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