Fully assembled 120Gb/s transceiver chips for high bandwidth density optical interconnects

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A complete 12X10Gb/s optical interconnect link, consisting of a novel fully assembled 12X10Gb/s transmitter chip and a fully assembled 12X10Gb/s receiver chip, will be shown in the paper. This new assembled approach utilized a thick photoresist ramp between CMOS driver and opto-electrical dies as the bridge for supporting co-plannar waveguides electrically plated with lithographic accuracy, which will allow for impedance matched metallic wiring between the electronic driving circuit and its opto-electronic counter part. The work is aiming to provide a quasi-wafer scale process for high bandwidth density, compact footprint and potentially low cost transceivers for future high-performance computing systems.

Introduction

As described in many papers [1-4], the performance of today's computer systems is limited by signal transport (data communication), rather than by the logic operation speed or memory capacity. Although, traditional copper wires are improving their performance by all kinds of techniques, such as active copper cable [5], still, these advances will not satisfy future interconnect requirements of bandwidth density and bandwidth distance product, due to the inherent limitation of the electrical wires [2].
Optics has improved bandwidth distance product and bandwidth density and if implemented in a cost effective-manner, optics may bring substantial system performance improvements [2]. Parallel optical interconnects is one of the best candidates for chip-to-chip interconnects. The transceiver-packaging concept based on 3D integration of the opto-electronic elements with the CMOS driver circuits offers the smallest footprint with high bandwidth, high density, low power, and low cost. Several projects have explored the use of vertical cavity surface emitting lasers (VCSELs) and photo-detectors (PDs) vertically stacked on the VCSEL drivers and TIA/LA CMOS chips to form parallel communication modules for data transfer [6-7]. They either use wire bonding for making the required electrical connections [6] leading to limited RF performance, or a novel Holey CMOS transceiver which had holes etched away into the silicon chip in a complicated process to allow for the use of flip-chip bonding [7].
In this paper, we report on the progress in 3D integration of transceiver modules. We will shortly review the new 3D stacking approach and a 12-channel 10Gb/s/ch transmitter based on the approach and then describe the required steps in integrating the 12-channel 10Gb/s/ch receiver module necessary for creating a full link.

3D stacking approach

Previously, we have proposed a novel 3D stacking solution [8]. An artist's impression of the method is shown in figure 1(a). The basic idea is to use a pick and place machine

to position the E/O dies on top of the CMOS wafer containing the complementary ICs (TIA chips for a photo detector array and laser drivers for a VCSEL array). Then, using a thick photoresist (PR) pattern to create a continuous ramp between the pads on the CMOS IC and Opto-electrical dies. Finally, an electrical-plating process is utilized to form the desired metal traces, which connect top and bottom pads on both ends of the PR ramp. In the former paper [8], we used this novel stacking method to demonstrate a 12-channel VCSEL array based transmitter, which is depicted in figure 1(b). As mentioned [8], it can be used widely as an efficient way to connect any fix paths of two quite different height surfaces on a wafer scale process, such as integration photodiode array with its counterpart CMOS IC. Figure 1(C) illustrates an artificial receiver model, which will be demonstrated in this paper.

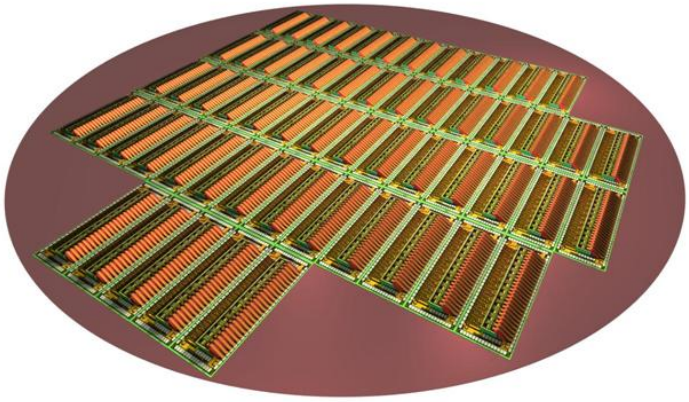

Fig. 1: (a) 3D stacking model demonstration

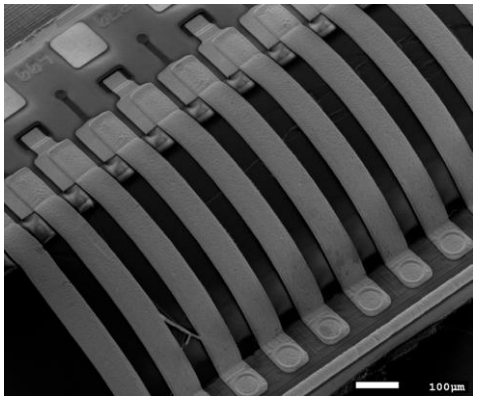

Fig. 1: (b) 3D stacking transmitter module

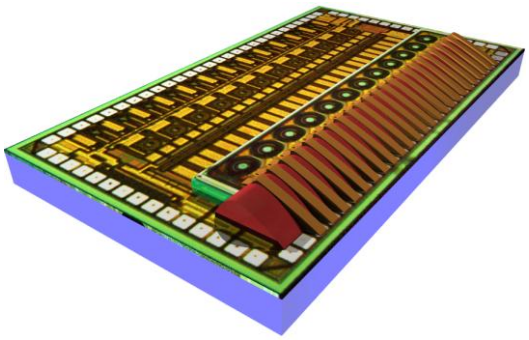

Fig. 1: (c) 3D stacking receiver artificial demonstration

3D stacking receiver fabrication

In the former experiment, the aluminium layer on the VCSEL driver pads has been attacked by the PR developer. Although the copper layer left on the driver pads can still make good electrical contact with metal probe for testing, it is less handy if wire bonding to a PCB evaluation board for module testing is desired. Thus, in the following experiment, we added post-CMOS process to prevent aluminium layer from being unnecessarily attacked.

Because the etch rate of silicon Nitride (SiN_X) in the developer is negligible, we introduce SiN_X as a protection layer. 100nm SiN_X layer is deposited on the TIA/LA CMOS IC surface. Then, a lithography step is used to define openings on the plating pads. The SiNx layer in these holes is etched away using dry etching as shown in figure

2. It can be seen that the rest of the TIA chip surface including the aluminum covered pads are still covered with SiNx until the last fabrication step. Sacrificing the aluminum layer on the plating pads is of no concern since the plated gold layer will be used for interconnecting these pads.

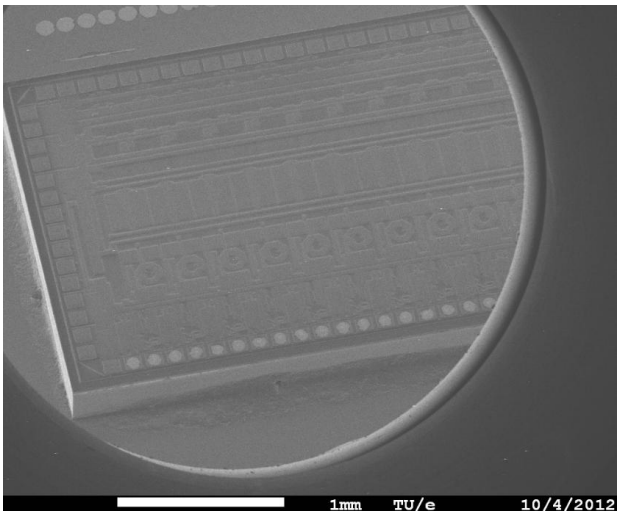

Fig. 2: After post-processing TIA/LA

Aside from this extra step the following process flow is similar to that carried out in making the transmitter chip [8]. In short, first the 12-channel 10Gb/s/ch. photodiode array die is placed on the TIA/LA chip, and is bonded with PR layer, as shown in figure 3(a). In the second step, a thick PR pattern is used to create a continuous ramp between the pads on the TIA/LA and photodiode array, as shown in the figure 3(b). Third step, another lithography step is used to define the plating area, the shape, the width, the length of the metal paths are controlled by lithography mask, shown in figure 3(c). In the forth step an electrical-plating process is used to form the desired metal traces, which connect top and bottom pads on both ends of the PR ramp, as shown in figure 3(d). The thickness of metal paths is decided by plating process. In this way every dimension of the interconnecting metal paths, shape, width, length and thickness are completely controlled. This flexibility allows to realize impedance matched metal traces between opto-electrical dies and CMOS IC, which is more and more essential at high data rate. Finally, the sample is put into the Nitride reactive-ion etching (RIE) machine to remove the SiNx layer.

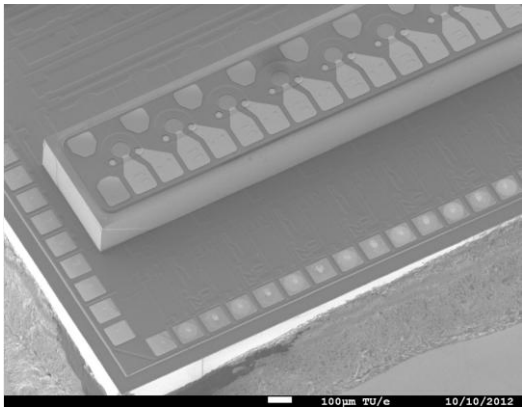

Fig. 3 (a) SEM image of photodiode array bonding on the TIA/LA CMOS IC

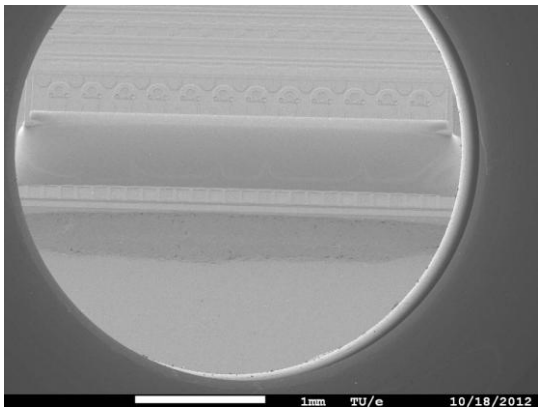

Fig. 3 (b) SEM image of photodiode array bonding on the TIA/LA CMOS IC

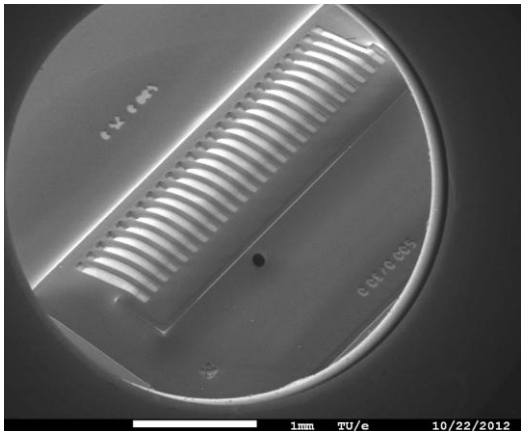

Fig. 3 (c) SEM image of the lithography between photodiode array and CMOS IC

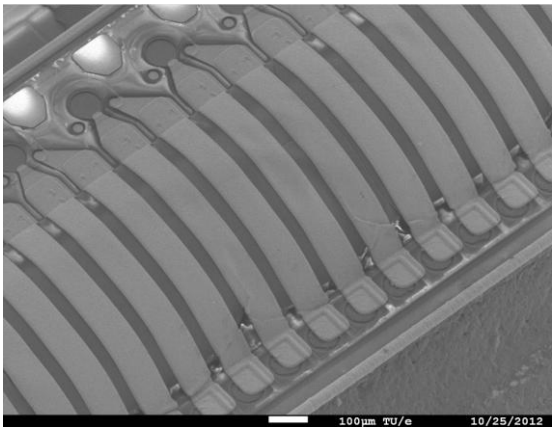

Fig. 3 (d) SEM image of the electrical path between PDs and CMOS driver IC

Conclusion

A receiver chip based on a novel 3D stacking approach was demonstrated in this paper. The method was used to stack a 200µm thick photodiode array die on the commercial TIA/LA CMOS IC. The PR ramp supported the metal traces, connecting the pads of the driver IC with those of the photodiode chip. The process is fully CMOS compatible, uses low temperature processes and can be applied on a wafer scale using low cost pick and place technology. The receiver module shown in this paper will be tested soon.

Acknowledgements

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