CMOS Compatible Heater Fabrication Approaches for Thermal Tuning of Photonic Devices

A. Masood[1], M. Pantouvaki[2], D. Goossens[2], G. Lepage[2], P. Verheyen[2], D. Van Thourhout[1], P. Absil[2], W. Bogaerts[1]

[1] Photonics Research Group (INTEC), Ghent University - imec, Department of Information Technology, Center for Nano and Biophotonics (NB Photonics), Sint-Pietersnieuwstraat 41, B-9000 Ghent, Belgium

[2]imec vzw, Kapeldreef 75, B-3001 Leuven, Belgium

adil.masood@intec.ugent.be

Thermal tuning is widely used method for precise wavelength selectivity in various integrated photonic devices. Since silicon photonics is gaining wider acceptance for communication and sensing devices, CMOS compatibility - in fabrication method as well as post fabrication integration – is gaining prominence. That makes it relevant to explore heater fabrication approaches for silicon photonics, which are highly compatible with CMOS and efficient in functionality. We present an overview of such different approaches currently being developed by us.

Introduction

Exponential rise in the performance of electronics devices has pushed electronics technology to its physical limits, specifically in the interconnect layers. Silicon photonics is perceived as the natural solution to this bottleneck [1]. This has led to efforts to explore material and fabrication technologies for silicon photonics devices which are compatible with complementary metal-oxide-semiconductor (CMOS) [2]. Using the same manufacturing platform for silicon photonics as CMOS electronics provides not only the better chances of integration with CMOS for optical interconnects but also possibilities of high-volume and low cost production [3][4][5][6]. Silicon has a relatively high thermo-optic coefficient of $1.86 \times 10^{-4}K^{-1}$, which greatly enhances thermal sensitivity of silicon photonics components [7]. This high thermal sensitivity makes devices prone to instable output due to external fluctuations, but it also provides opportunity to thermally tune wavelength selective filters [8]. There is a great variety of Joule's heating based heaters for thermal tuning in photonic devices like doped silicon slabs [9], metal lines [10] and metal silicide lines [11]. From the above discussion, it can be stated unequivocally that a CMOS compatible silicon photonics device requiring thermal tuning must be complemented by heaters which are CMOS compatible as well. We can ascribe following attributes to define CMOS compatibility: no impact on photonics functionality; similarity to CMOS back-end processing and room for further high level integration and packaging [12].

In this paper, we present four different kinds of Joule's heating based tuners, which completely fit the definition of CMOS compatibility stated above. These heaters were fabricated using four different fabrication technologies on the same photonic test vehicle so that their performance can be benchmarked.

Device Design and Fabrication

A Mach Zehnder Interferometer (MZI) was chosen as the test vehicle for measuring heater performance. If a section of one arm of MZI is heated, it can cause a change in refractive index for the heated section of the waveguide. This then results in a phase

shift $\Delta\phi = 2\pi L/\lambda \times \Delta T \times \beta$, where $\Delta\phi$ is the change in phase, L is length of the heated section, λ is the wavelength of the optical signals, ΔT is change in temperature of the waveguide and β is the thermo-optic coefficient of the waveguide material i.e. silicon.

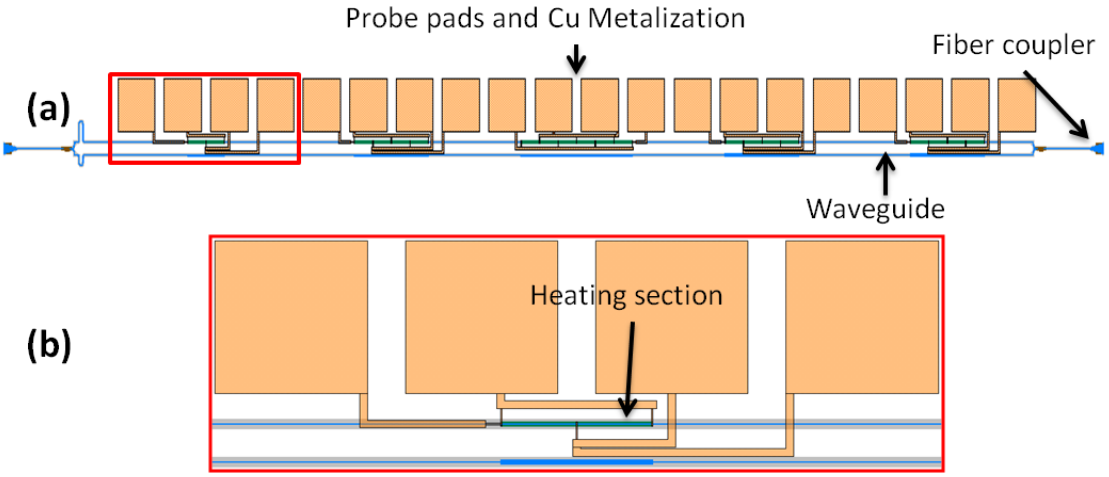

Figure 1: (a) MZI with five heating sections and its probe array. (b) 4-probe configuration for heating section

In this case, an unbalanced MZI with 2.55mm long straight arms was designed. This long length was used to place 5 heating sections on one of its arms with different heater parameters like width and spacing (see Figure 1). A 4-probe configuration was chosen for driving the heating sections and for accurate resistivity measurement. The pads were realized in the metal 1 level (copper). Passive photonic components were fabricated on 220nm Silicon-on-Insulator (SOI) wafers using the standardised silicon photonic platform at imec vzw, Belgium [13]. Following this step, standard CMOS modules were used for doping implants, metal silicidation, overlay oxide, contact plugs and metal 1. These modules have been successfully used previously for fabricating modulators and heaters on photonic devices [12][14].

The next four sections describe the different technologies used for realizing the heaters.

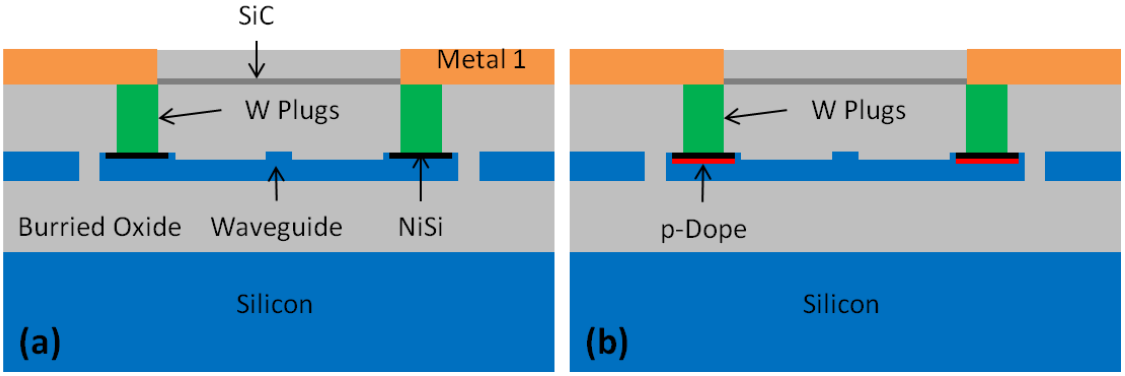

Figure 2: (a) NiSi heater cross-section; (b) p-Doped silicon heater cross-section

Ni – Silicide Heater

Metal silicides provide a low contact resistance to gates in CMOS and their fabrication process is standard. It involves infusing metal ions on silicon for silicidation. The same process can be used to make long lines of metal silicides. In this case, we made long lines of Nickel Silicide (NiSi) and connected them to metal 1 using tungsten (W) plugs

at two ends (Figure 2(a)). Two NiSi lines have been implemented parallel to the waveguide.

Doped Silicon Heater

Doped silicon is conductive and can be used for Joule's heating, similar to resistive metal lines. Figure 2(b) shows a cross section, which is similar to the cross section for the NiSi heaters. However, in this case NiSi is deposited only at the bottom of the W plugs and not as lines. Hence, on electrical contacting, current flows parallel to the waveguide through the doped region. The doping concentration is kept at around $1 \times 10^{18}/cm^3$.

Doped Waveguide Heater

Doped waveguide heaters enable the flow of electric current through the waveguide in the direction perpendicular to the wave propagation. That enables heating of the core directly. As shown in Figure 3(a), the waveguide is doped with p implants. To reduce the contact resistance, p+ doping (higher implant concentration) is performed beneath the W plugs. In this design the core is heated directly but the doping of the waveguide may result in higher optical losses.

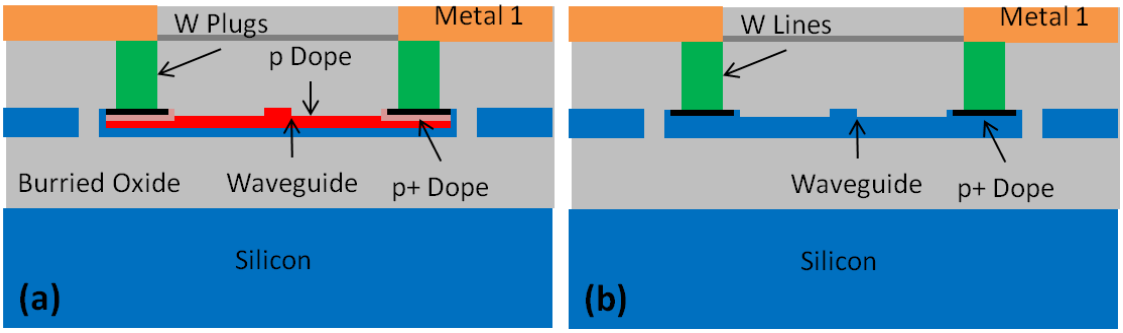

Figure 3: (a) Doped waveguide heater cross-section; (b) Parallel metal line heater

Parallel Metal Line Heater

In this heater design, the W plugs (which are cylindrical in shape) are replaced by long trenches in the same layer and filled with W. These lines are contacted at their ends, causing electric current to flow in parallel to the wave propagation. These trenches are very large in cross section and hence require a larger power consumption to cause heating.

Measurements

These four types of heaters have been implemented on different types of waveguides. Also, a parametric sweep on heater width and heater offset from the waveguide has been implemented. Below we present one set of measurements giving comparative results between the different heaters. It shows the power requirement for shifting half free spectral range (FSR) i.e. π shift of the MZI (FSR = 11.8nm). All four heaters were on shallow waveguide with 100µm of heating length:

NiSi	Doped Si	Doped Waveguide	Parallel Metal
27.3mW	23.7mW	26.5mW	193.2mW

As expected, the parallel metal heater consumes maximum power. Results for the other three compare to similar heaters available in literature. Note these results are coming from a single device and have not been adjusted to remove energy loss in metal 1, probe contact etc.

Further Work and Conclusion

Current results are indicative for the general trend but it is expected that an exhaustive measurement of the full parametric sweep will provide more accurate numbers on the heater performance. Heaters with performance similar to those reported in literature were fabricated using standard CMOS back-end modules.

References

[1] P. Bettotti and L Pavesi, "Nanosilicon photonics as a platform to widen the scope of silicon photonics" in International Conference on Information Photonics (IP), pp. 1, 2011.

[2] R. Soref, "Silicon photonics: A review of recent literature", Springer Silicon, Volume 2, 1-6, 2010.

[3] L. Tsybeskov, D.J. Lockwood, and M. Ichikawa, "Silicon photonics: CMOS Going Optical", Proceedings of the IEEE, Volume: 97, Issue: 7, pp. 1161-1165, July 2009.

[4] C. Kopp, S. Bernabe, B. B. Bakir, J-M. Fedeli, R. Orobtchouk, F. Schrank, H. Porte, L. Zimmermann, and T. Tekin, "Silicon photonic circuits: On-CMOS integration, fiber optical coupling, and packaging", IEEE Journal of Selected Topics in Quantum Electronics, Volume 17, Number 3, May/June 2011.

[5] W. Bogaerts, P. Absil, D. V. Thourhout, J. V. Campenhout, S. K. Selvaraja, P. Dumon, H. Yu, A. Masood, G. Roelkens and R. Baets, "Optical interconnect technologies based on silicon photonics", 2011 MRS Spring Meeting, Volume 1335, 2011.

[6] P. Dumon, W. Bogaerts, R. Baets, J-M. Fedeli, L. Fulbert, "Towards foundry approach for silicon photonics: silicon photonics platform ePIXfab", Electronics Letters, Volume: 45, Issue: 12, pp. 581-582, 2009.

[7] G. Cocorullo, "Thermo-optical modulation at 1.5mu in silicon etalon", Electronics Letters, Volume: 28, Issue: 1, pp. 83-85, January, 1992.

[8] W. Bogaerts, S.K. Selvaraja, P. Dumon, J. Brouckaert, K. De Vos, D. Van Thourhout, R. Baets, "Silicon-on-Insulator spectral filters fabricated with CMOS technology", IEEE Journal of Selected Topics in Quantum Electronics, Volume: 16, Issue: 1, pp. 33-44, January-February, 2010.

[9] J. Song, Q. Fang, T. Liow, H. Cai, M. Yu, G. Lo, and D. Kwong, "High efficiency optical switches with heater-on-slab (HoS) structures", in Optical Fiber Communication Conference, pp. 1-3, March, 2011.

[10] D. Dai, L. Yang, and S. He, "Ultrasmall thermally tunable microring resonator with a submicrometer heater on Si nanowires", Journal of Lightwave Technology, Volume: 26, Issue: 6, pp. 704–709, 2008.

[11] J. V. Campenhout, W. M. J. Green, S. Assefa, and Y. A. Vlasov, "Integrated NiSi waveguide heaters for CMOS-compatible silicon thermo-optic devices" Optics Letters, Volume: 35, Issue: 7, pp. 1013-1015, 2010

[12] A. Masood, M. Pantouvaki, D. Goossens, G. Lepage, P. Verheyen, D. V. Thourhout, P. Absil, and W. Bogaerts, "CMOS-compatible tungsten heaters for silicon photonic waveguides", in Proceedings of 9th International Conference on Group IV Photonics, pp.234-236, 2012.

[13] S. Selvaraja, P. Jaenen, W. Bogaerts, P. Dumon, D. Van Thourhout, and R. Baets, "Fabrication of photonic wire and crystal circuits in silicon-on-insulator using 193nm optical lithography", Journal of Lightwave Technology, Volume: 27, Issue 18, pp. 4076-4083, 2009.

[14] H. Yu, M. Pantouvaki, J. V. Campenhout, K. Komorowska, P. Dumon, P. Verheyen, G. Lepage, P. Absil, D. Korn, D. Hillerkuss, J. Leuthold, R. Baets, and W. Bogaerts, "Silicon carrier-depletion-based mach-zehnder and ring modulators with different doping patterns for telecommunication and optical interconnect", in 14th International Conference on Transparant Optical Networks (ICTON), pp. 1-5, 2012.