Monolithic Integration of a InP Nano-laser on (001) Si Substrate

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A unique epitaxy process has been developed to grow high quality InP nanowires on (001) Si substrates. By optical pumping, room temperature lasing has been successfully achieved and a large spontaneous emission factor is obtained, indicating strong confinement of the optical mode in the cavity.

Introduction

As the microelectronics manufacturers keep shrinking transistor sizes and manage to integrate more and more devices on a single chip, the bottleneck that limits the overall system performance becomes the conventional copper based interconnects. In the meantime, optical interconnect is attracting more and more attention, and the evolution of the underlying technology strongly supports the anticipation that optical interconnects will become a competitive solution for overcoming the intra- and inter chip communication bottleneck [1, 2]. As the key component for an optical communication system, however, a high performance on-chip laser source is still missing. Different approaches are being actively explored across the world. For instance, extensive work is being carried out nowadays to engineer silicon or germanium for optical gain generation [3, 4]. Nevertheless, III-V materials are still the best option, considering their superior performance and the technology that has been developed for decades. Wafer bonding based integration techniques were proposed for III-V on silicon integration and resulted in considerable success over the last decade [5, 6]. On the other hand, although the more appealing monolithic approach is challenging for implementation, considerable progress has recently been made.

Among various solutions, localized epitaxial approaches, e.g. the growth of III-V nanowires on silicon, have shown remarkable progress [7, 8]. However, most of the demonstrated growth processes were carried out on a (111) silicon surface, making it not compatible with the advanced complementary metal-oxide-semiconductor (CMOS) infrastructure. In addition, due to the limited dislocation-free lateral dimensions of the III-V nanowires grown on silicon, the integration approach normally utilized is to grow relatively wide III-V nanowires on a III-V wafer as the first step, and then a complex cleavage and transfer process is employed to integrate the Fabry-Perot nanowire cavity on a silicon wafer [9, 10]. A more controllable growth scheme is needed to increase the low yield and high cost associated with the approach mentioned above. In this work, a new approach is proposed for growing relatively thick InP nanowires on a pre-defined (001) silicon substrate. Without any complex post-processing, InP nano-lasers are successfully integrated on silicon by using a metal-organic chemical vapor deposition process (MOCVD). Under pulsed optical pumping, low threshold room-temperature laser operation is successfully achieved.

Experimental

Different from the recently demonstrated InGaAs laser on silicon, whereby the growth was preceded by a surface roughening process [11], we start the epitaxy selectively within 100 nm diameter sized circular openings that were defined in a 350 nm thick SiO_2 mask on a (001) silicon substrate. The definition of these SiO_2 patterns was carried out in a standard CMOS fab, using a modified shallow trench isolation process (STI) [12]. A schematic of the process flow of the epitaxial growth can be found in Fig. 1(a).

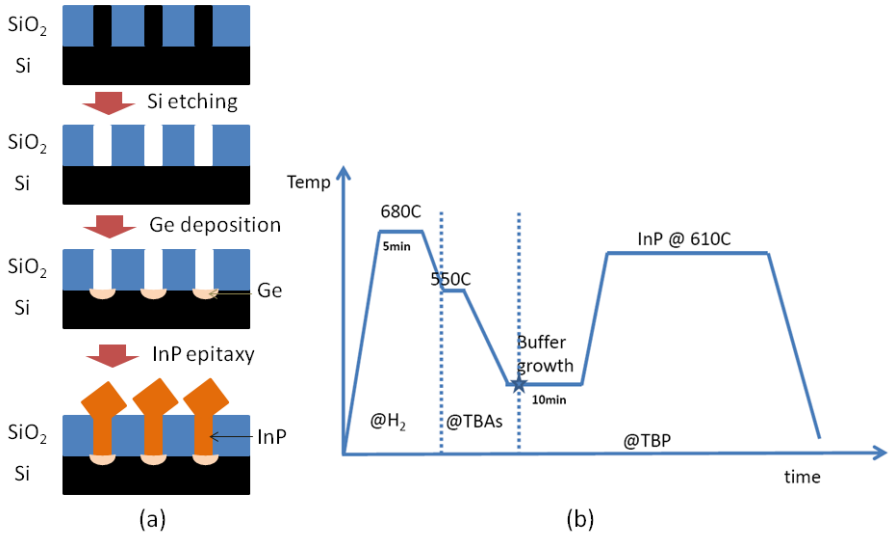

Figure 1. (a) Process flow for the InP MOCVD growth on the STI templates and (b) the growth thermal cycle for InP growth.

After etching the silicon channels by HCl at high temperature (600°C) in a CVD reactor, a thin Ge seed layer is deposited. The Ge layer is used to reduce the lattice mismatch between silicon and InP, while after a subsequent high temperature (680 °C) annealing in a H_2 flow, the Ge surface will form appropriate steps for better InP nucleation, reducing the generation of anti phase boundaries (APBs)[13]. As presented in Fig. 1(b), in the next step, the MOCVD reactor temperature is reduced to 380 °C and low flow rates Tertiarybutyl phosphine (TBP) and Trimethylindium (TMI) are introduced for the InP nucleation. After 10 minutes of InP growth, the reactant flow rates are increased while the temperature is increased to 610 °C, and the main part of the InP growth starts. By making the STI trenches narrow (aspect ratio > 2), all the dislocations that propagate from the lattice mismatched interface will be annihilated at the trench sidewalls, because dislocations normally glide along certain angles respect to the (001) surface [13].

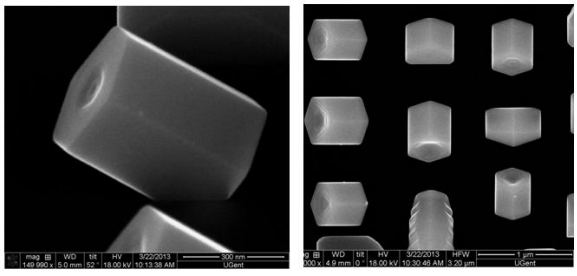

Figure 2. (a) A tilted scanning electron microcopy (SEM) view of a typical nano-laser cavity and (b) a top view of the nanowire array grown on (001) silicon substrate

In such a way, dislocation-free InP is obtained at the top part of the STI trenches, and the subsequent growth is carried out on this virtual lattice matched substrate. In the later epitaxial growth above the SiO_2 mask surface, nanowires with a diameter of about 400 nm are formed. A typical scanning electron microscopy (SEM) image of an InP nanowire on silicon can be found in Fig. 2(a). Similar to most of the works reported in literature, the obtained nanowire is oriented along the <111> axis, with a hexagonal cross-section. In Fig. 2(b), we also present a SEM image of the sample surface in a larger scale to show the yield of the epitaxial growth. Nanowires are found to be oriented along four equivalent <111> directions. Due to the close distance between the pre-defined SiO_2 holes, failure to grow a certain nanowire affects the surrounding nanowires, resulting in different growth dimensions. This is mainly due to the loading effect of the epitaxial growth and it provides a way to control the wavelength of the nanowire laser, i.e. by controlling the nanowire dimensions through the careful design of the surrounding mask.

Characterization Results

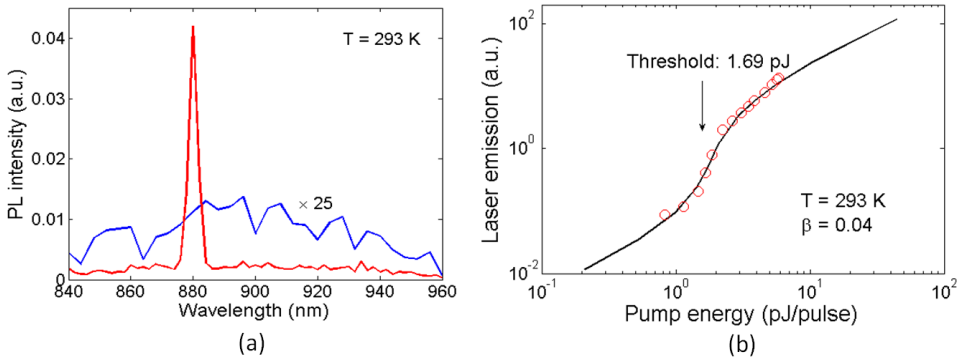

Figure 3. (a) PL emission spectrums recorded below (blue) and above (red) the threshold. (b) Light in – Light out curve of a nano-laser (open circles are measured results, and solid curve is the rate equation fitting)

Using a micro-PL setup, room-temperature lasing behavior has been achieved from these InP/Si nanowire cavities. A Nd:YAG nanosecond pulsed laser (Ekspla, 532 nm, repetition rate 321 Hz) was used as the pump source, and the collected PL signal was detected through a ¼ m monochromator (MS257, Newport) by a TE-cooled silicon detector. The signal-to-noise ratio was improved by using a lock-in amplifier.

A typical laser emission spectrum from a signal nanowire cavity can be found in Fig. 3(a). The PL spectrum below threshold (magnified by a factor of 25) is also plot as a reference. As one can see, by increasing the pump intensity, a laser peak located around 880 nm can be clearly identified (see the red curve). The relatively wide linewidth, which is routinely found in literature for micro-cavity based lasers, is mainly due to the large spontaneous emission factor β. The spontaneous emission and stimulated emission rates are increased considerably so that the carrier distribution is largely distorted and extra noise is introduced [14, 15]. In Fig. 3(b), the collected PL emission of the lasing peak as a function of the input pump energy is presented on a logarithmic scale (red open circles). The clear transition proves the laser exhibits threshold behavior. A low threshold of 1.69 pJ is derived. By performing a standard rate equation fitting, a large β

of around 0.04 is extracted, which indicates that a large portion of the spontaneous emission is coupled into the lasing mode. It supports the hypothesis for the large linewidth discussed above.

Conclusion

In summary, a unique epitaxial scheme was developed and relatively thick InP nanowires with good material quality were successfully integrated on pre-defined (001) silicon substrates without any complex post-processing. Pulsed lasing from these nanowires has been obtained at room temperature with a low threshold. The demonstrated laser may find a role in the application field of on-chip optical interconnects.

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