Fabrication technology of metal-cavity nanolasers in III-V membranes on silicon

V. Dolores-Calzadilla,[1] E. J. Geluk,[1] T. de Vries,[1] B. Smalbrugge,[1] P. J. van Veldhoven,[2] H. Ambrosius,[1] D. Heiss,[1] A. Fiore,[2] and M. Smit[1]

COBRA Research Institute, Eindhoven University of Technology,
Postbus 513, 5600 MB Eindhoven, The Netherlands.
[1] Photonic Integration, Department of Electrical Engineering
[2] Photonics and Semiconductor Nanophysics, Department of Applied Physics

Electrically pumped metal-cavity nanolasers in III-V semiconductors are promising for their application in optical interconnects, where high integration density and low optical powers are required. They offer a low threshold current and excellent cooling properties due to the metal encapsulation. In this contribution, an overview about the technology required for the fabrication of a nanolaser coupled to an InP-membrane waveguide on silicon is presented. A variety of techniques are used including electron-beam lithography, dry and wet etching, as well as deposition of dielectrics and metals. The technological challenges to fabricate such a complex nanostructure are also discussed.

Introduction

Metal-cavity semiconductor nanolasers were recently demonstrated experimentally. This new type of lasers are interesting in view of their potential characteristics, which include high integration density, excellent cooling properties, ultra-fast modulation, etc, which make them attractive for low power applications such as optical interconnects. First devices showed lasing at cryogenic temperatures [1], and lasing at room temperature was achieved later [2]. These devices radiated into the far field. For their integration in photonic circuits waveguide coupling is mandatory, which increases their fabrication process complexity.

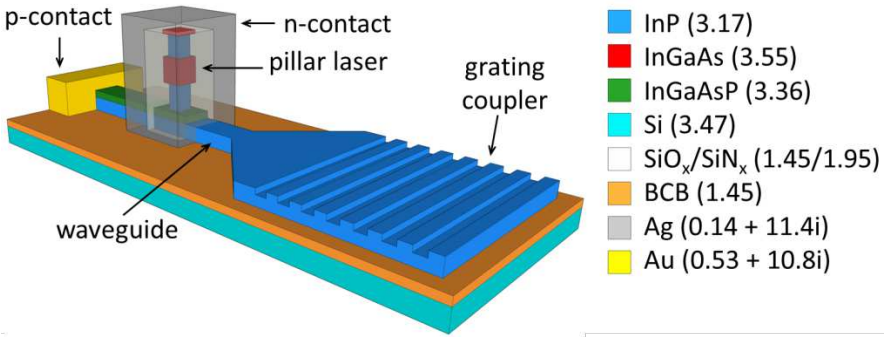

Figure 1. Schematic of a metal-cavity nanolaser coupled to an InP-membrane waveguide connected to a grating coupler. The refractive index of each material at 1.55 µm is shown in parenthesis.

We propose a metal-cavity nanopillar structure coupled by evanescent field to an InP-membrane waveguide as shown in Fig. 1 [3]. Both the laser and waveguide are fabricated in a III-V layer stack bonded to a silicon substrate with Benzocyclobutene (BCB) [4]. The pillar has an undercut above and below the active region (InGaAs) to increase the cavity quality factor. It is covered by a dielectric layer and then encapsulated with silver to form the metal-cavity that provides a strong feedback to the

TE mode supported by the cavity. The metal cladding makes electric contact on the top of the pillar, whereas a lateral p-contact is deployed over a large area to minimize its contact resistance. For characterization purposes, we include a grating coupler to couple the light out of the chip.
The present contribution gives an overview of the fabrication technology of this nanolaser, that we are presently developing. The most relevant and critical fabrication steps are discussed, as well as the challenges that have to be met.

Electron-beam lithography and etching processes

The definition of the nanostructure is carried out by electron-beam lithography (EBL) due to the high resolution required. This is done in three EBL steps. During the first lithography, the nanopillar is defined. Later, an overlay exposure is needed to define the waveguide and, finally, the grating coupler is defined with another overlay exposure. Three different lithographic masking schemes are used during these EBL steps, which are depicted in Fig. 2(left) and discussed in the following.
The first EBL exposure is done using HSQ resist, which is a negative resist well known for its usage in high resolution lithography [5]. Since it can be thinner than 100 nm, the influence of the electron scattering inside the resist is limited. Nevertheless, its thickness is not enough to etch a hardmask able to withstand the etching of the pillar (about one micrometer high), and therefore it has to be used in combination with another resist in a bilayer resist scheme in order to be able to etch high aspect ratio structures [6]. The pattern in HSQ is transferred to an underlying HPR504 resist by means of a reactive-ion-etching (RIE) process using oxygen, which in turn is used to transfer the pattern into a SiO_x layer with a CHF_3-based RIE. Finally, the SiO_x is used as a hardmask to etch the semiconductor pillar using inductively coupled plasma RIE (ICP-RIE) using a methane-hydrogen chemistry (CH_4:H_2).

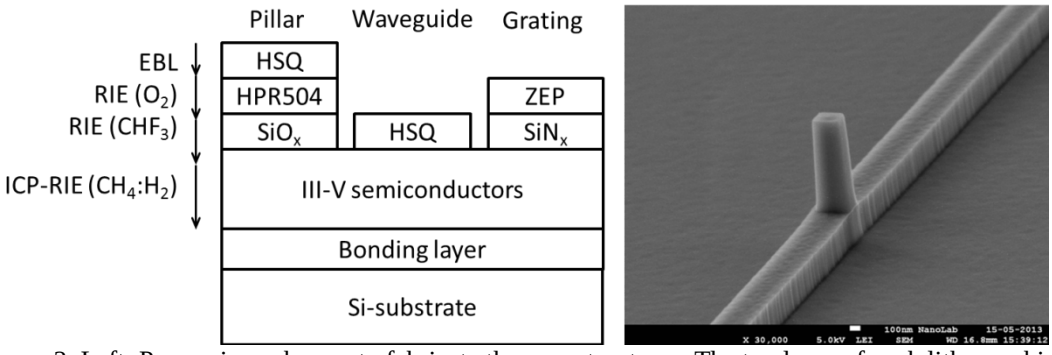

Figure 2. Left: Processing schemes to fabricate the nanostructures. The top layer of each lithographic scheme is always defined by EBL and development. Right: Pillar after waveguide etching and removal of hardmasks.

In a second EBL exposure, the waveguide is defined at the bottom of the pillar structure. During this step, a mask protection for the pillar is mandatory, otherwise the pillar will be eroded during the waveguides etching. For this purpose, the hardmask to etch the pillar is not removed after the first lithography.
An overlay EBL normally demands a prior planarization of the surface to keep the resist thickness uniform as well as the hardmask layer. We avoid such planarization by using the HSQ resist directly as the hardmask. This technique requires enhancing the resistance of HSQ to the semiconductor etching chemistry used in the RIE, what can be

done either by hardly curing HSQ [7] or by treating it with an oxygen plasma [8]. In this way, after the pillars have been etched, HSQ is spun, e-beam exposed, developed, and treated with an O_2-plasma. Later, this HSQ is used as the hardmask to etch the waveguide using methane hydrogen in a RIE process. The result of these two lithography steps is shown in Fig. 2(right).
A final e-beam lithography is required to fabricate the grating coupler. In this case, ZEP resist in combination with a SiN_x mask is used. This is preferred because it is a positive resist, which means that any non-exposed region (i.e. the pillar and waveguide) will be protected by the SiN_x hardmask during the grating etching. The undercut to enhance the quality factor of the cavity, as described in our laser design [3], can be fabricated right after the pillar etching by a selective wet etching of InP as it is shown in Fig. 3.

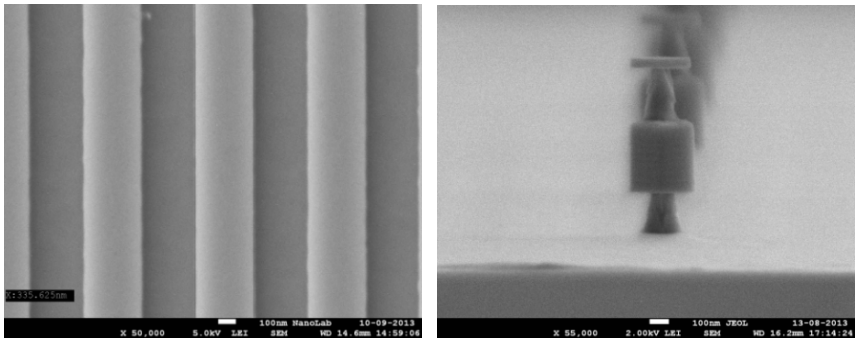

Figure 3. Left: Top view of a typical grating coupler. Right: Pillar with undercut fabricated using the solution H_2O:H_3PO_4:HCl.

Deposition of dielectrics and metals

The metal cladding of the cavity would create a short circuit unless a dielectric layer is deposited before silver, which also helps to reduce the metal loss according to the design [3]. For this purpose, either SiN_x or SiO_x can be deposited by plasma-enhanced chemical vapor deposition (PECVD), however it has been found that a SiO_x cladding would result in a higher quality factor due to its lower refractive index. Before the actual deposition of the chosen dielectric, a thin passivation layer of SiN_x of a few nanometers can be deposited at low temperatures to reduce the surface recombination [9]. Since the resonant wavelength is mainly given by the cavity size (thickness of the dielectric cladding plus the semiconductor pillar width), it is important to consider that the PECVD deposition rate on sidewalls is about two thirds of the deposition rate on a flat surface.
After the pillar has been covered with a dielectric layer, silver can be thermally evaporated to form the metal-cavity. However, since silver does not stick on SiO_x/SiN_x, an adhesion layer must be previously deposited by lift-off, for example Ti/Au [1], chromium [10] or germanium. In order to properly cover the sidewalls of the pillar, the silver evaporation should be done at different angles. Moreover, since the evaporation leads to the formation of silver grains, rapid thermal annealing (RTA) is applied after the evaporation to increase the metal grain size resulting in a more uniform metal with reduced scattering loss. Figure 4 shows a pillar covered with silver before and after RTA.

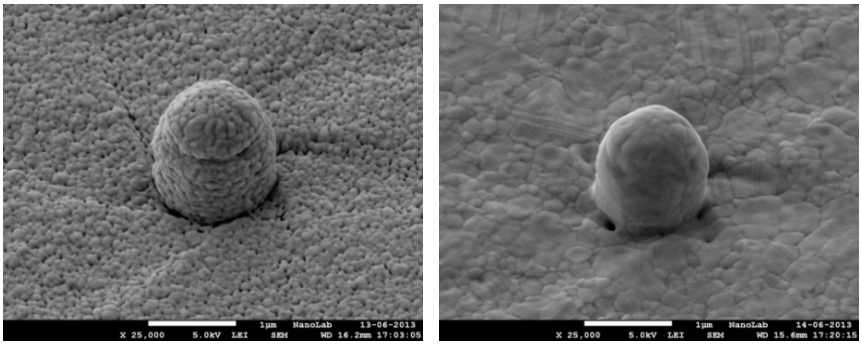

Figure 4. Left: Pillar after silver evaporation. Silver grains of about 30 nm are formed. Right: Silver-covered pillar after RTA.

Conclusions

A general overview of the processing technology to fabricate waveguide-coupled metal-cavity nanolasers in InP-membranes bonded to silicon has been presented. The most critical fabrication steps have been presented, which can also be used for other metal-based nanophotonic circuits.

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