Silicon CMOS Integrated Nanophotonics for Optical Interconnects

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The promise of CMOS Integrated Silicon Nano-Photonics (CINP) is to bring the low-cost manufacturing infrastructure, high capacity, and high functional yield traditionally associated with the semiconductor industry to the space of short-reach optical interconnects [1]. Today, this need is being driven by emerging large volume applications in datacenters, supercomputers, and wireless antenna backhaul, which require cost-effective, power efficient, and scalable optical transceivers, operating at data rates up to and exceeding 25 Gbps. This trend is in direct contrast to the traditional long-haul fiber optic communication market, where low volumes of high-cost transceivers (often employing advanced modulation formats, coherent detection, dense WDM, and power-hungry digital signal processing) are utilized to transmit data at petabyte-per-second rates along single-fiber optically amplified channels. Accordingly, the short-reach optical interconnects market drives a very different set of device/sub-system design and manufacturing constraints.

Silicon photonics technology, which enables intimate integration of analog, digital, and mixed-signal circuits together with optical components such as modulators, photodetectors, and wavelength division multiplexing filters, is a viable approach for significantly decreasing the cost of optical transceivers, facilitating their massive deployment in large scale systems. This technology manifests itself in several different stages of development. Available solutions range from the hybrid approach which separates electrical and optical functions between completely separate chips, to a fully monolithically integrated solution where all functionality (aside from the laser source) is designed and fabricated on a single silicon chip. In the ideal case, this would encompass the manufacture of complete opto-electronic systems in one continuous monolithic integration flow, and would include the adaptation of established high-throughput automated chip packaging methods to incorporate a light source and attach fibers to the silicon photonic die. Both approaches each have their pros and cons.

This talk will provide an overview of IBM's 90nm CMOS Integrated Silicon Nano-Photonics technology, which realizes monolithic integration of deeply-scaled high-speed optical circuits within the front-end of a standard CMOS process. Recent advancements in integrated components for modulation, switching, photodetection and fiber-to-chip packaging will be presented.

References

[1] Y. Vlasov, IEEE Communications Magazine, February issue, S67-72, 2012.

[2] S. Assefa et al., "A 90nm CMOS Integrated Nano-Photonics Technology for 25Gbps WDM Optical Communications Applications," International Electron Devices Meeting (IEDM), post-deadline paper 33.8, December 2012.