A new packaging approach for transceiver modules: Embedding the bare dies into PCB*

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Transceiver modules are considered to be essential building blocks for high bandwidth density optical interconnects. In order to reduce the cost and simplify the fabrication process, a new packaging approach will be discussed in this paper. Instead of integrating chips on a silicon carrier, a PCB with well-patterned metal traces will be utilized and two areas on the PCB will be cut as holes to reserve the space for the chips. Following this, the chips will be flipped into the holes and the bare dies will be connected to the pads on the PCB and finally a molded optics interface will be used to couple the laser into the optical fibers. The fabrication process will be completely, reliably and accurately controlled by machines.

Introduction

Optical interconnects have become one of mostactive disciplines in the field of optical communication in last few years [1] and it has been shown that the density of transceiver is a critical limitation for the size of switches and the number of hosts that can be connected to a switch [2]. Compared with traditional copper wire, optical interconnects have many advantages such as high bandwidth density, high data rates, small footprint and low power consumption [3]. As a result, electrical links have been successfully replaced by optical links in high-performance application domains. Also, it has been shown that individual and parallel optical links based on VCSELs offer small power dissipation (less than 0.1pJ/bit/m), low-drive current, high-speed modulation properties, and high wall-plug efficiency. For those reason VCSEL based transceivers have been widely used in many fields such as data centers, switching and routing systems and local area networks [4]. However, current available transceivers based on VCSELs also have several drawbacks as they are expensive and contain many complicated fabrication and assembly processes [3,5,6]. This high-cost of technology limits their penetration. Therefore, many efforts have been taken to solve this problem. A 2009 paper indicated that the cost of optics will decrease from $10/Gbps in 2008 to $1.1/Gbps in 2012 and decline to $0.17/Gbps and $0.025/Gbps in the year of 2016 and 2020 respectively [7]. Embedding the bare dies into PCB is one of the most promising solutions, which can be used to simplify the fabrication processes and reduce the cost.

In this paper, we will discuss a new packaging approach for transceiver modules. This approach allows bare dies to be directly embedded into PCB without the need of any interposers. Using the proposed approach, a low-cost and simple assembly is made possible. The process can be reliably and accurately controlled by machines.

* PCB: Printed circuit board

The Concept of Design

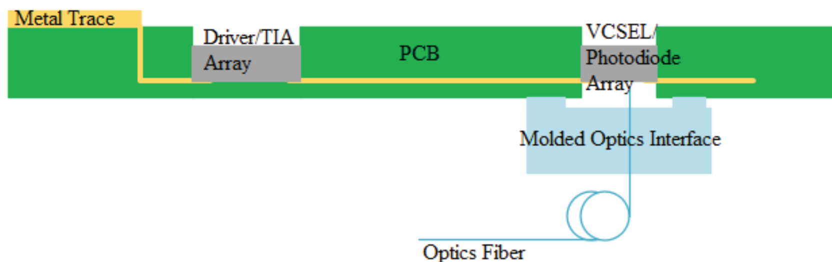

Figure 1Schematic cross-section view of the transceiver module

Figure 1 shows the schematic cross-section view of the transceiver module. For a transmitter, the electronic signal can be transported into the flipped VCSEL driver array and VCSEL array through differential traces in a PCB. A molded optics interface can be used to keep alignment and couple the laser from the VCSEL array into fibers. For a receiver, the optical signal from an optical fibers can be accurately detected by the photodiode array with the help of molded optics interface then amplified by the TIA/LA array. After that, the metal traces on the PCB can be used to deliver the differential signal to the edge of card connector.

Schematic Fabrication Processes

The process steps are schematically illustrated below.

Figure 2 PCB preparation

Figure 2 presents the PCB material which should be used. Firstly the layers of the PCB are patterned with the metal traces and pads, which are used to connect the ICs and other components. The size of PCB board should be as large as the final mid board optics or pluggable optics solution and include the edge of card connector if needed. The geometry of traces on PCB also should satisfy the differential condition of the ICs in order to reduce the reflection caused by the impedance mismatching. Such mismatches may result in unwanted attenuation of signal and eventually increase the power consumption.

Figure 3 Cutting step of PCB

As shown in figure 3, two holes are cut in the PCB to allow the placement of the bare dies. These holes are prepared for the VCSEL driver or TIA/LA array and the VCSEL or photodiode arrays. This step can be done by wet etching, laser cutting or any other suitable process depending on the material of the PCB. The holes need to be large enough for the bare dies to fit inside but not too large to allow freedom of movement, which may causes problem in alignment process.

Figure 4 Assembly of flipped chips in PCB

A VCSEL driver array and a VCSEL array (or a TIA/LA array and a photodiode array) are placed in the holes etched in the PCB (figure 4). The ICs should be flipped so that the bare dies connect to the metal pads on the PCB directly. The distance between the pads on the bare dies is typically 125 µm, which means that the pads and traces on the PCB also should have the same pitch. This process can be carried out with a fully automated pick and place machine to ensure sufficient placement accuracy. After that, the ICs need to be soldered either by a reflow process or by any other suitable process.

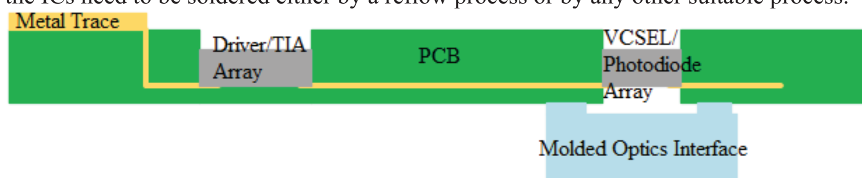

Figure 5 Alignment with a molded optics interface

In figure 5, a molded optics interface is placed on the bottom of the PCB. Automated pick and place machines are also used in this step in order to make the precise alignment between the molded optics interface and the markers drawn on the bottom of silk screen layer. The function of this process is to accurately couple the laser from VCSEL array (optics fibers) into optics fibers (photodiode array). This molded optics interface can be glued or fixated by laser welding, depending on the material of PCB and molded optics module.

Simulation and Discussion

The design of high-speed inputs, which involves 100 Ohm differential impedance, is a critical challenge in this approach due to the small feature of pads and traces on the PCB. As mentioned above, the distance between the pads should be 125 µm. Therefore, the design of differential transmission line is simulated by ADS software package to check for its feasibility.

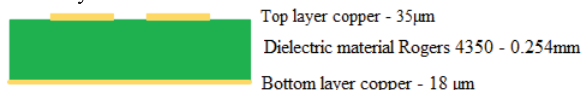

Figure 6 the cross-section view of micro strip transmission line

The cross-section view of micro strip transmission line used in the simulation can be shown in figure 6. The thickness of copper layer on the surface and inner are 35 µm and 18 µm respectively. Between the two copper layers is a dielectric material Rogers 4350B, which is 0.254 mm thickness.

Figure 7 depicts the simulation results of transmission coefficient S_{21} parameter. According to figure 7(a), the propagation loss of trace with 65 µm width and 60 µm spacing is only 0.3 dB/cm, while the propagation penalty of trace with 50 µm width and

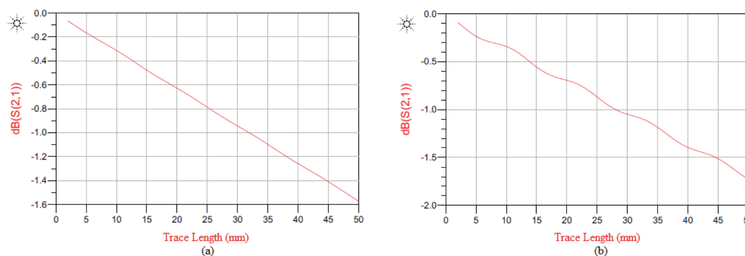

Figure 7 Simulation results of S21 parameter at 10 GHz of (a) trace width = 65 µm, spacing =60 µm (b) trace width = 50 µm, spacing = 75 µm

75 µm is also acceptable. This means that current PCB technology can indeed be used to implement the assembly concept discussed above.

Conclusion

In this paper, we have suggested a new packaging approach for transceiver modules. In the approach, a PCB with well-patterned metal traces was used to replace silicon/glass carriers used in previous work and the bare dies were embedded directly into the PCB. This approach requires only several fabrication processes, which are completely, reliably and accurately controlled by machines, and requires no wire bonding, which leads to cost reduction. Moreover, the same packaging process can be used if the number of channels increases or if the bit-rate increases, which shows a huge potential. Due to the simplified fabrication processes, this approach will present a clear way to design and fabricate low-cost transceivers.

Acknowledgement

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