

## **Fabrication of an efficient metal grating coupler for membrane-based integrated photonics**

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*This paper reports the progress on the fabrication process of highly efficient metal grating couplers for membrane-based integrated circuits, using double side processing technology on bonded samples. This type of gratings comprises a buried SiO<sub>2</sub>/Ag grating of 125nm thickness with a silver layer as metal mirror, and has several advantages over dielectric gratings as metallic gratings are independent from the buffer thickness. We predict a theoretical chip-to-fiber coupling efficiency of 74% and 89% for uniform and apodized gratings respectively, at a wavelength of 1550 nm. Furthermore, the fabrication process can be used for both, SOI and III-V based platforms.*

### **Introduction**

Coupling light in and out of a photonic integrated circuit (PIC) is needed for device characterization and performance evaluation. Such coupling of light can be done by end-fire coupling or via grating couplers. In membrane-based photonic platforms no lenses or spot size converters are needed due to the grating's capability of mode matching from photonic wires to a fiber. Regarding membrane-based platforms, the technological development of complementary metal-oxide semiconductor (CMOS) has made silicon on insulator (SOI) a natural choice for passive circuits. On the other hand, InP-membranes on silicon (IMOS) have been proposed as an approach to combine both, passive and active components in a single photonic platform [1].

Grating couplers can be used in both platforms, they are comprised among the devices useful for on-wafer characterization, optical interconnect systems that requires coupling in chip-to-fiber and chip-to-chip schemes [2] among other applications. However, a usual performance limitation of such gratings is the power leakage to the substrate and free space diffraction [3]. Many efforts have been done to increase the performance of the grating couplers efficiency and to have broadband operation; both, with dielectric and metal-based devices. It is of interest for this research the metal-based designs where the use of metals allows for higher efficiency to the optical fiber by decreasing the losses due to substrate leakage.

An outstanding design is a metal layer placed at the bottom of the buffer layer to reflect the diffraction to the substrate. This design can achieve a coupling efficiency up to 78% [4]. Another design is based on the fabrication of a metal grating on top of a waveguide by lift off showing an efficiency of 60% and 1 dB bandwidth of 40 nm [5]. Despite the increase on coupling efficiency, these metal grating designs depend on the buffer thickness under the photonic membrane. More recently in 2012 P. Lin presented a design in which the grating efficiency is independent of the buffer layer thickness by means of a photonic band-gap effect [6]. However, the grating grooves require being 600

nm thick. This is clearly a disadvantage since it is very challenging to fabricate such a grating by lift off.

In this paper we present how we overcome those weaknesses by a novel metal grating design which is explained in the following section.

## Design

We propose a metal grating coupler designed for TE polarization which comprises buried  $\text{SiO}_x$  stripes followed by a metal gating and a metal mirror layer to inhibit power leaking into the substrate. This device is compatible with silicon on insulator (SOI) and InP-membranes. The design proposed here results in a highly efficient grating coupler independent from the buffer thickness and with the advantage of using well known standard fabrication processes [3].

The flexibility of the device can be seen from its freedom to either use a thin bonding layer useful for heterogeneous integration of III-V materials and silicon photonics [7], or a thick bonding layer useful for thermal isolation between a photonic membrane and an underlying CMOS circuit, with maximum efficiency in both cases.

The design parameters for maximum efficiency of the metal grating coupler calculated by 2D FDTD simulations are as follows:  $\lambda=1.55 \mu\text{m}$ , coupled to a fiber (core  $9\mu\text{m}$ ) at 10 degrees and  $10\mu\text{m}$  away from the grating, period  $\Lambda=635 \text{ nm}$ , groove depth (of  $\text{SiO}_x$ )  $d=125\text{nm}$ , waveguide width= $400 \text{ nm}$ , waveguide thickness= $250 \text{ nm}$ . Theoretically a maximum efficiency of 74% is achieved with these parameters.

## Fabrication

The proposed metal gratings are based on double side processing, being defined the gratings on one side and the waveguides on the other side, after bonding. The layer stack consist of an InP membrane of 300 nm thickness bonded to silicon by a 50 nm thick layer of  $\text{SiO}_x$  on top of a Benzocyclobutene (BCB) layer of 600 to 900 nm thickness.

Four e-beam lithography (EBL) steps are needed. Figure 1 shows the schematic of 2<sup>nd</sup> and 3<sup>rd</sup> EBL in the top left part, followed by the 4<sup>th</sup> EBL after bonding in bottom left. The right part of the figure shows a 3D view of the buried metal gratings with a tapered waveguide of InP on top.

The first EBL defines the marks for further alignment through all the process. For this EBL step ZEP resist 520A (320 nm thick) is used on top of a  $\text{SiNx}$  layer of 300 nm which works as a hard mask for the dry etching on the ICP (Inductive Coupled Plasma) machine. The patterned marks are transferred by reactive ion etching in the  $\text{SiNx}$  layer and afterwards, etched in the semiconductor layer by ICP with depth of 650 nm. The  $\text{SiNx}$  mask is removed with BHF (Buffered Hydrofluoric Acid).

For the second EBL step the sample is prepared by depositing a 125 nm thick layer of  $\text{SiO}_x$  with PECVD (Plasma-enhanced Chemical Vapor Deposition), followed by the spinning of ZEP resist 520A (320 nm thick). The patterning for the second EBL consists of the gratings with the specifications of the design. After development, the gratings are

etched with reactive ion etching into the  $\text{SiO}_x$  and the residual resist is removed by oxygen plasma. The result of the  $\text{SiO}_x$  stripes is shown in a SEM picture in Figure 2A.

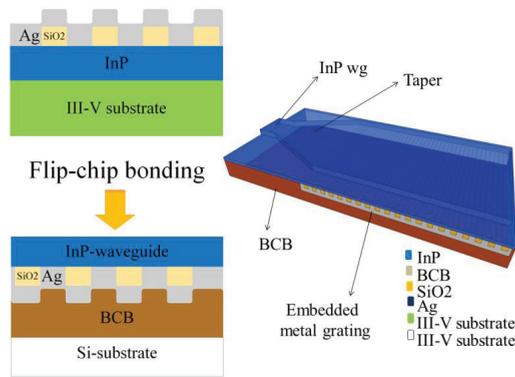


Figure 1. Schematic flow of metal-gratings fabrication and 3D view.

The third EBL comprises the metal liftoff. In this EBL step the sample is prepared by spinning PMMA 495 resist A11 (790 nm thick) covering the  $\text{SiO}_x$  gratings. The EBL patterns pads with the size of the gratings dimensions (20 by 15  $\mu\text{m}$ ) in order to cover just those regions with metal and leave the rest of the wafer clean. Right after the development, a very thin layer of 2 nm of germanium (Ge) followed by 300 nm of silver (Ag) are deposited with e-beam evaporation without breaking vacuum between the two evaporation processes. The Ge acts as sticky layer for the Ag on top of the  $\text{SiO}_x$ . The Lift off is then performed submerging the sample to one hour of acetone vapor followed by one hour of liquid acetone and rinsed afterwards with acetone and propanol. Top view of the metal gratings is shown in Figure 2B.

After the third EBL is performed, the sample is bonded into silicon with a thick BCB layer of 600 to 900 nm.

In the last EBL step the tapered waveguides are patterned on top of the buried metal gratings. The tapers used are 250  $\mu\text{m}$  long and 15  $\mu\text{m}$  wide, and the 400 nm wide waveguides vary from 100  $\mu\text{m}$  to 1 mm in length to allow characterization of waveguide losses.

For this last EBL, a 100 nm thick layer of  $\text{SiN}_x$  is deposited in the wafer, followed by spinning of ZEP resist 520A. After development, the waveguides are etched into the  $\text{SiN}_x$  and then, into the InP membrane (300 nm thick) by means of ICP. It is important to leave footage of 50 nm to avoid reaching the bonding layer. An exposed bonding layer is attacked by BHF and HF, which is used afterwards to wet-etch the  $\text{SiN}_x$  mask. Figure 2C shows the SEM picture of the tapered waveguides on top of the buried metal gratings.

## Outlook and conclusions

First samples have been fabricated and measured with losses of 6.5 dB per grating and an efficiency of 25%. The performance has not yet reached the theoretical values

because of known fabrication issues which will be solved in a second fabrication run later this year.

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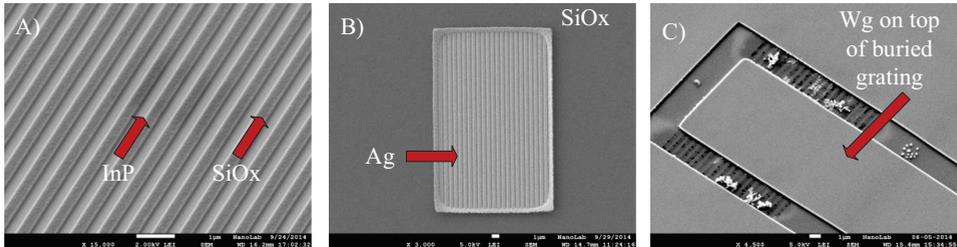


Figure 2. SEM pictures of the gratings fabrication process. Top left shows patterned  $\text{SiO}_x$  gratings (2<sup>nd</sup> EBL), top right shows gratings covered with Ge and Ag (3<sup>rd</sup> EBL). Bottom center shows the tapered waveguide patterned on the InP membrane over the buried metal gratings (4<sup>th</sup> EBL).

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