Demonstrating efficient design transfer methods for complex photonic integrated circuits

A. Sosa,[1] K. Welikow,[2] R. Broeke, [3] A. Bakker,[2] D. Tsiokos,[4] T. Tekin,[1] and N. Pleros [4]

[1] Technische Universität Berlin, Research Center of Microperipheric Technologies, Gustav-Meyer-Allee 25, 13355 Berlin, Germany
[2] PhoeniX Software, Hengelosestraat 705, 7521 PA Enschede, the Netherlands
[3] Bright Photonics, Burgemeester van den Helmlaan 67, 3604 CE Maarssen, the Netherlands
[4] Aristotle Univerisity of Thessaloniki, Information Technologies Institute - Center for Research and Technology Hellas, P.O. Box 114, 54124 Thessaloniki, Greece

We designed an Indium-Phosphide-based Access Point Module photonic chip for 60GHz FTTH wireless applications, using a Multi Project Wafer run for two different foundries. In our submission we will closely examine the applied design methodology, starting with the required functionalities, and then defining the building blocks of the chip and preparing the final mask layout. Until recently, this last step was done independently for each foundry, but with the use of generic photonic building blocks in the applied design environment, the migration between different foundries is facilitated, and therefore the efficiency of our design cycle is increased.

Introduction

Today's microphotonics presents a fragmentation regarding the number of integration technologies and optimization methods that depend on a specific application. This prevents the application-specific Photonic Integrated Circuits (ASPICs) [1] from reaching a low-cost industrial volume manufacturing process and gaining wider interest in the market. Therefore, microphotonics experts have established standardized building blocks (BBs) [2] that allow the manipulation of basic light properties, such as amplitude, phase and polarization. This enables the generic integration process for the design of advanced circuits and systems. However, to move forward design processes and standardized technologies must be taken into account. This will enable the development of design libraries and software infrastructures that will permit designers to use certain components and predefined subcircuits. Using this method we will obtain an increase in efficiency of the design process, therefore obtaining the desired performance and decreasing the design cycles. In this paper we demonstrate the improvement of the design process using such a dedicated software infrastructure, permitting an effective design transfer between foundries of an essential ASPIC for the COMANDER [3] project. This project is funded under the Marie Curie IAPP and has as a main objective the deployment of a fully converged Next-Generation Fiber-Wireless network architecture that provides: simultaneous fixed and mobile access; unforeseen multi-Gbps transmission speeds in the wireless domain; extended coverage Local Area Networks; interconnection of wired and wireless nodes at the MAC layer and; enhanced resource utilization features by employing advanced Network Coding techniques.

Multi-Project Wafer runs

Through the generic integration technology we can combine several designs in a single wafer through a standardized generic process to generate ASPICs. These wafers are called Multi-Project Wafer (MPW) runs [2], and by implementing them, new

comers will be able to enter rapidly into the market. The MPW runs will lead to a reduction in the volume of applications, but for its execution it is indispensable the use of an automation tool to streamline chip runs for foundries, and to allow the production of PICs in a first-time-right environment [4].

Generic Foundry Model

A chip manufacturer that provides open access to its generic integration process is considered a generic foundry [1]. This model shows to be promising in the microphotonics world, especially for Indium Phosphide (InP) based generic foundries [5][6] since this material is currently the only type that enables integration of optical gain (or amplification) blocks, an essential feature of onchip integrated optical sources. The InP- wafer runs are being coordinated by the JEPPIX broker [6], in which experts in this field cooperate. InP-based generic foundry processes are offered at the moment by 3 manufacturers: Oclaro in the UK, Fraunhofer Heinrich Hertz Institut (HHI) in Berlin and SMART Photonics in the Netherlands.

Photonics Design Automation

A Photonic Design Automation oriented flow (PDAFlow) (Fig. 1), for design and manufacture, requires the use of foundry specific process design kits (PDKs) [1] with component libraries that contain the mask layout of the BBs to design ASPICs. However, the design must also pass through the foundry's design rule verification (DRC) to ensure that the design is foundry compliant. The PDAFlow [1][4] starts by defining the specs required to obtain a level of performance on the system level, so the designer can then determine the required BBs; if certain BBs are not provided in the PDKs, they can be modeled by using light propagation simulators. The combination of both sets of BBs can then be simulated using a circuit simulator to determine the overall behavior of the chip. Later on it will be passed to the foundry, where it will take into account the process flow and deliver the results that will run through the foundry's software. The PDAFlow's concept is the base for the Integrated Product Creation Process (iPCP) (Fig. 2) [4]. The iPCP describes the process of interaction between all the stakeholders: system engineers, design engineers, and process engineers; through the use of software, or standard interface, that delivers an efficient and error free transfer of designs between different software packages.

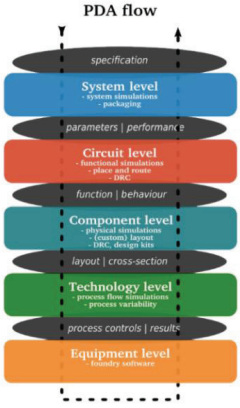

Figure 1. Photonics Design Automation Flow.

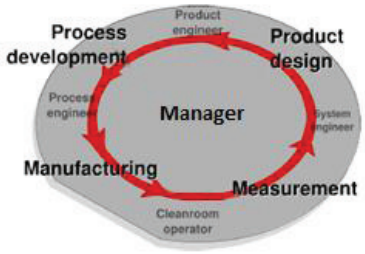

Figure 2. Integrated Product Creation Process.

Demonstration of Design Transfer

Thanks to the similarity of certain BBs across PIC platforms we can perform a design transfer between different foundries without producing major changes in the performance of the chip. However, these similar BBs can present notorious changes in the footprint on the mask layout as a consequence of the different processes that are used in the foundries in question. Initially we had as a goal the transfer of a PIC design, with one application, between two foundries (HHI and Oclaro). The InP platform was used for the MPW run delivered by the PARADIGM [7] project, where two designs are run per project to compare platforms.

We used OptoDesigner 5 (OD5) [8] with the foundry provided PDKs and IP-Block extensions [9]. OD5 is equipped with a template based design for die and package, and allows us to maintain, in its majority, the same script, and to make a design transfer just by modifying these two aspects. In our designs, the package used was the same in both cases, GoochHousego, but the die was modified, hhiDieBB and oclrDieBB. OD5 also performs a mask cross section (mcs) post processing, in which the HHI waveguide definition maps to multiple Graphic Data System (GDS) layers with different under-etch corrections, and the Oclaro waveguide definition uses inversion, but thanks to the foundry's maintained PDKs this is fully hidden from the designer.

To determine which BBs are transferable, we must follow a design flow in which from the proposed application we determine the functionality that the ASPIC must have. Afterwards, we check the available BBs from each foundry and determine all attractive possibilities to meet such functions. If the possible BB options do not overlap between foundries the transfer cannot be made. In our case, the absence of certain BBs, like Oclaro's EOPM, or HHI's DBR laser, did not permit the transfer of all BBs, but we were still able to maintain the same functionalities in both designs.

Our ASPICs purpose is to be employed as an optical subunit of an Access Point Module (APM) developed on the COMANDER project. The APMs optical subunit employs a Coarse Wavelength Division Multiplexing (CWDM) demultiplexer in order to separate the optical signal into six spectral areas. The first two bands reserved for FTTH signals, the following two used for the data signals between APM and Central Office (CO) on Radio over Fiber (RoF), and the last pair intended for the MT-MAC control signals. To carry out all these functions a complex chip is required with the use of many BBs, of which the BB that stands out for its importance since it is designed as the CWDM demultiplexer is the AWG [9]. Thanks to the AWGs joint implementation with OD5, it allows a flexible configuration and has an adaptable simulation runtime via the use of the PDAFlow, therefore, generating a GDS file with the correct optical and geometrical specifications.

The AWG was first designed in HHI using an IP-Block in OD5; it was optimized to obtain a flattened output and the desired spectral arrangement. By changing certain factors in the script, such as, the foundry PDK, and any other foundry specific parameters; we were able to simulate the same AWG for the Oclaro foundry. We obtained a large difference in the footprint of the mask layout (Fig. 3); the HHI AWG occupied an area of approximately 2.5x1.5 mm^2, and the Oclaro AWG an area of 1.5x1.0 mm^2. Regarding the spectral response (Fig. 4) the results were slightly different, but similar enough that it was within our grasp to center transmitters and receptors (FTTH, RoF, CTR) from both foundries at the same wavelengths, proving that the design transfer was successful.

We also used several generic px-elements [8] (pxMMI, pxSinebend, and more) which are easily transferable BBs. These elements incorporate an adaptable feature, such as, the automatic use of tapers to adjust the width of the input/output waveguides of the BBs as it occurs with the MMI. Another px-element that has this feature is the SOA that is defined on a shallow etched level and therefore may require the use of a waveguide transition element that will be placed automatically.

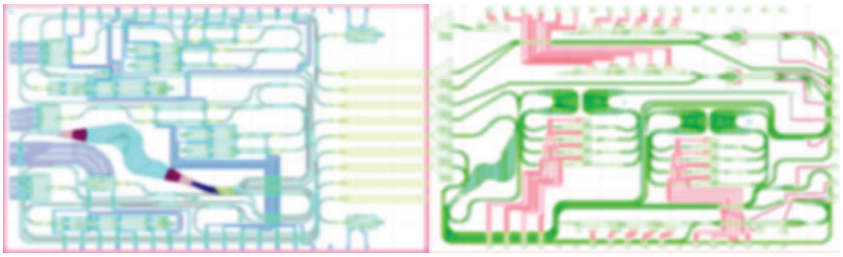

Figure 3. Mask Layout for HHI foundry (left), and for Oclaro foundry (right). Both 6x4 mm²

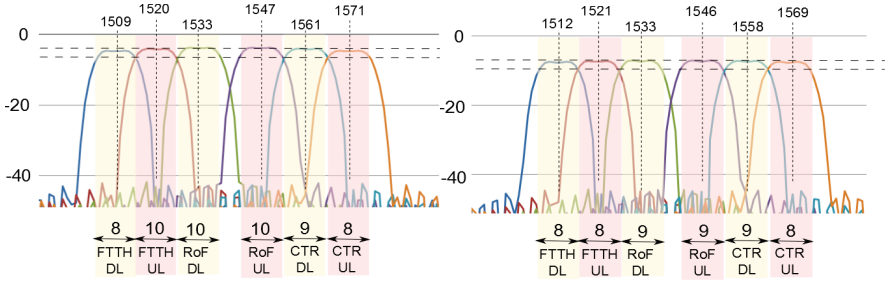

Figure 4. AWG spectral arrangement of CWDM DEMUX
for HHI foundry (left), and for Oclaro foundry (right)

Conclusion

We described a design environment for the design transfer of a single complex PIC between two platforms. For BBs that are similar on both platforms we demonstrated BB transfers on a one-to-one basis. Some BBs are not directly transferable due to the different platform technologies. For those we made a transfer with composite BBs at the functional level instead. By combining both transfer methods we obtained two chips with similar functionalities on the two different platforms. This design approach can be extended to other platforms as well.

References

[1] M. Smit et al"Generic foundry model for InP-based photonics"IET Optoelectr, vol. 5,187-194, 2011.

[2] M. Smit, et. al., "An introduction to InP-based generic integration technology," IOP Semicond. Sci. Technol., vol. 29 (5), pp. 41, 2014.

[3] COMANDER Project- http://www.mc-comander.eu

[4] T. Korthorst, et. al., "Photonic Design Automation," NASA TechBriefs, Nr. 23, 2013.

[5] D. Robbins, K. Lawniczuk, and M. Smit, "A generic process platform for photonic integrated circuits," SPIE Newsroom, 2014.

[6] InP MPW brokering organisation: JePPIX - http://www.jeppix.eu

[7] PARADIGM Project - http://paradigm.jeppix.eu/

[8] PhoeniX Software OptoDesigner 5: http://www.phoenixbv.com/optodesigner

[9] Bright Photonics - http://www.brightphotonics.eu