

Diffraction-suppressed adiabatic tapers for photonic circuits

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Tapers are indispensable elements in photonic integration since they allow for general mode and spot size conversion. Adiabatic tapers are preferred for low losses and large tolerances. The most widely used taper shapes are linear and parabolic. In this contribution we present a taper shape, based on a Gaussian approximation to inhibit the diffraction. This results in the shortest possible taper for a specified (high) efficiency conversion. Consequently, it reduces substantially the footprint of photonic devices using tapers. Fabrication in an InP-membrane platform and characterization results are presented.

Introduction

Tapers are widely used in photonic circuits for mode and spot size conversion regardless of the photonic platform employed. Among the most interesting applications of tapers in photonic circuits nowadays are: grating couplers, spot size converters for edge coupling, laser out-coupling in the heterogeneous integration of III-V and silicon photonics, etc. When the taper length is not a concern, typically long linear or parabolic tapers are used which guarantee a smooth mode conversion. Nevertheless, for applications where the footprint is of key importance, tapers are required to be as short as possible.

In this contribution, we present an adiabatic taper with a shape such that high mode conversion efficiency is achieved by suppressing the propagation diffraction similar to the design proposed in [1], nevertheless our design is based on a Gaussian optics approximation which results in a more accurate description. In the next section, the design considerations and simulations of a two-dimensional taper structure are discussed. Fabrication and characterization results are presented in the third and fourth sections, respectively, and then the conclusions are given.

Design

For simplicity, we limit ourselves the design of a short taper whose width varies from 400 nm to 2 μm as shown in Fig. 1a. The results are however applicable to tapers connecting waveguides of arbitrary width. We confirm this by showing simulation results of a taper with final width of 10 μm , which is a transition of special interest in photonic membrane circuits to connect a photonic wire with a grating coupler to allow in- and out-coupling with an optical fiber.

Since most of the planar photonic circuits are typically simulated in a two-dimensional space, we perform the design using 2D Finite Difference Time Domain (FDTD) simulations and a mode solver.

An adiabatic transition is such that the optical power remains in the fundamental mode. This could be achieved if the phase front remains flat as the mode propagates, thereby preventing the excitation of high order modes. Since diffraction is responsible for the phase front curvature, efficient mode conversion could be achieved if diffraction is suppressed.

In order to suppress the diffraction by means of the taper shape, we assume that the light propagation in a slab region can be described by Gaussian optics. As the light enters in an homogeneous slab, it will tend to diffract at the divergence angle θ_d , given for Gaussian beams as $\theta_d = \lambda/n_{eff}\pi w_0$, where λ is the wavelength in vacuum, n_{eff} is the effective mode index and w_0 is the beam waist radius. In a taper, such diffraction is reduced if the local taper angle is lower than the divergence angle.

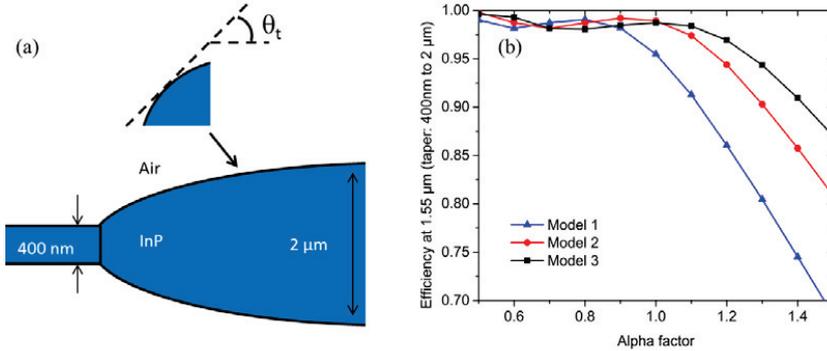


Figure 1. (a) General schematic of the simulated adiabatic taper. (b) Taper efficiency of a linear, parabolic and the proposed models for diffraction suppression as a function of α factor.

From this description, a design rule follows for adiabatic tapers with suppressed diffraction: the taper angle should be at any point smaller than the divergence angle of the propagating light. It means that

$$\theta_t < \alpha \frac{\lambda}{n_{eff}\pi w_0}$$

, where θ_t is the local taper angle and α is a factor close to unity that accounts for the Gaussian approximation made.

We consider three different design models: (1) n_{eff} varies along the taper and w_0 is measured where the intensity drops by a factor of $1/e^2$ according to Gaussian optics theory, (2) n_{eff} varies along the taper and $w_0 = w_t/2$, where w_t is the taper width, and (3) n_{eff} has a fixed value corresponding to the highest value it can take (i.e. at the widest taper section) and $w_0 = w_t/2$. The first model matches the theory better, whereas the third description simplifies the design since only a single simulation with a mode solver is required. Figure 1b shows the simulation results for the three different models, and for different α -values. High transmission efficiency is achieved when $\alpha \leq 0.9$, $\alpha \leq 1$ and $\alpha \leq 1.1$, for the three models respectively.

In the case of a taper varying from 400 nm to 10 μm , an efficiency of 98% is obtained when using model (3) with $\alpha = 1$. For comparison with other taper shapes, we simulated a linear and parabolic tapers with the same length (78 μm), resulting in an efficiency of 91% and 97%, respectively. Although the efficiency achieved with the parabolic shape approaches to the diffraction-suppressed shape, it is worth to highlight that a series of simulations are typically required to optimize the taper length for a given case. On the other hand, our proposed model automatically results in the shortest adiabatic taper connecting two arbitrarily wide waveguides for a specific wavelength, since it is based on physical reasoning.

Fabrication

Diffraction-suppressed adiabatic tapers were fabricated on an InP membrane on silicon (IMOS) platform [2] using the model (3) mentioned in the previous section with the highest $n_{eff} = 2.62$. The membrane is a 250 nm thick InP layer bonded with Benzocyclobutene (BCB) polymer to a 1.8 μm thick layer of SiO_2 on a Si wafer. The fabrication process is based on two electron-beam lithography (EBL) steps with high resolution required. Two different lithographic masking schemes were used during these EBL steps. These are depicted in Fig. 2.

The first EBL, which corresponds to the waveguides and tapers definition, has been carried out by using Hydrogen silsesquioxane (HSQ) as negative tone resist material and hard mask for the subsequent etching process. This technique requires enhancing the resistance of HSQ to the semiconductor etching chemistry used in the Reactive-Ion Etching (RIE), which can be done either by curing hard HSQ [3] or by treating it with oxygen plasma [4]. In this way, after HSQ was spun, e-beam exposed, developed, and treated with an O_2 -plasma, it is used to etch the waveguide and tapers using a methane hydrogen chemistry ($\text{CH}_4:\text{H}_2$) in a RIE process.

The second EBL is required to define the grating couplers for input and output coupling. A scheme of ZEP resist in combination with a SiN_x layer is used for this purpose. ZEP is preferred because it is a positive resist where only the exposed pattern will be open, leaving the rest of the sample protected by SiN_x during the etching.

For our experiment, we fabricated two chips. In both samples stitching errors were present. These errors lead to extra losses on the devices which are not possible to extract from our measurements. This compromises the measurements of performance of the tapers. Actions need to be taken to solve these errors and further improvements in the fabrication of these devices will be implemented in our next fabrication run.

Characterization

We characterized several mode converter pairs sets for each α factor. Each set has a different number of tapers in order to obtain the insertion loss per taper from a linear dependence. To eliminate the effects of the waveguide loss, we designed the same

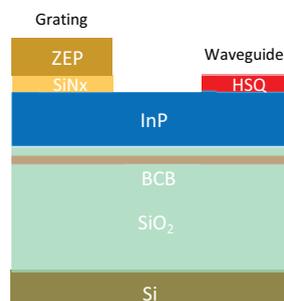


Figure 2. Lithography mask schemes used to fabricate the waveguides and the gratings.

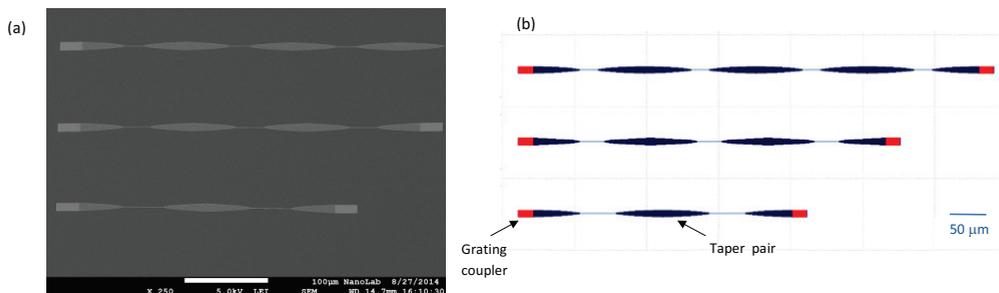


Figure 3. (a) SEM picture of the set of tapers fabricated. (b) Lithography mask of the devices and the input/output gratings.

length of waveguide ($L_{wg} = 100\mu\text{m}$) for each set, adjusting the distance between the pairs of tapers. In this way, the measured losses will in principle just comprise the transition loss and the propagation loss of each taper. Fig. 3a is a Scanning electron microscope (SEM) picture of the fabricated devices and Fig. 3b is the lithographic mask of the fabricated devices.

In order to characterize our samples, the light has been in- and out-coupled to the chip with the grating couplers, designed to work for the TE mode. The gratings are illuminated with optical fibers angled 10° with respect to the chip surface. The incoming light passes through a polarization controller to set the TE mode.

From every set of devices we measured the transmitted power and calculate the losses per taper. Fig. 4 shows the fraction of transmitted power for each set of tapers for different α factors. Due to the problem with stitching errors, the measurements include extra losses which are not possible to isolate. Nevertheless, the general behaviour of the transmission efficiency versus the α factor can be observed. It is important to note that for $\alpha > 1$, the efficiency drops dramatically.

Even with the extra losses, tapers with a $\alpha \leq 1$ have a transmission higher than 95 % (less than 0.22 dB losses) which indicates that without the stitching errors, we can expect good performance adiabatic tapers close to our simulated results.

Conclusions

An adiabatic taper shape based on a Gaussian approximation to inhibit the diffraction was proposed which allows for a simple and quick design of high efficiency tapers (up to 98%) based on a single mode solver calculation. The characterization measurements were compromised by stitching errors in the fabrication, nevertheless the general taper behaviour has been observed and transmission efficiencies exceeding 95% were observed for $\alpha \geq 1$. A new fabrication run is under way in order to get more definitive results.

Acknowledgements

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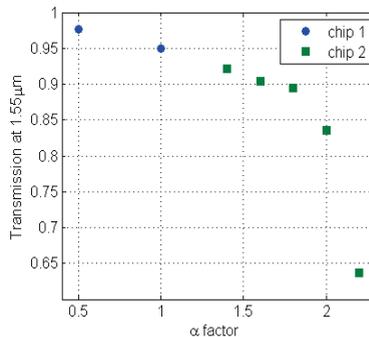


Figure 4. Taper transmission as a function of α factor. Circle marks are measurements from chip 1; square marks correspond to measurements from chip 2.