

A novel approach of integrating III-V on the silicon nitride platform

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Heterogeneous integration of III-V semiconductor materials on the silicon platform is one of the most promising methods for the fabrication of active devices in silicon photonics. In order to implement this method also on the silicon nitride platform, we propose a new type of spotsize converter that uses amorphous silicon as an intermediate coupling layer. This new method is shown to have a high tolerance to bonding and lithography misalignment. While the minimal coupling loss between the III-V and the silicon waveguide lends itself to applications that require power efficiency.

Introduction

Silicon photonics, leveraging the well-developed CMOS fabrication infrastructure and its economy of scale, is emerging as a powerful technology for the integration of optical functions on a chip. However, the realization of an efficient laser on silicon remains a serious challenge because of silicon's indirect bandgap. This requires the integration of III-V semiconductor lasers on the silicon photonics platform. The classical integration approach involves either fiber pigtailling an external laser [1] or attaching a micro-packaged III-V laser [2] to the silicon circuit using active alignment techniques. While these are viable solutions for the integration of single laser diodes, these approaches don't scale well.

On the silicon-on-insulator (SOI) platform, heterogeneous integration has been developed to tackle this issue, either based on direct [3] or adhesive [4] bonding. The tolerance to large bonding misalignment and simple packaging means that this technology is suitable for low-cost and high-volume applications with a high number of lasers. The minimal coupling loss between the laser and the silicon waveguide lends itself to applications that require power efficiency. Moreover, the direct integration between materials permits the realization of a bunch of new functions, like laser cavities in the silicon layer.

In recent years silicon-nitride-on-insulator is emerging as a promising material platform, which is transparent in the 400-5000 nm wavelength range. Owing to a lower refractive index contrast than silicon, much lower losses can be achieved in silicon nitride (Si_3N_4) waveguides. Moreover, Si_3N_4 has a lower thermal coefficient than silicon and is therefore less prone to thermal fluctuations. Since silicon nitride circuits can also be fabricated in a CMOS fab, they inherit the same advantages as the silicon-on-insulator waveguide platform.

However, heterogeneous integration of III-V materials on the silicon nitride platform leads to more complicated design, making it more susceptible to fabrication intolerance [5]. The fundamental issue is the low refractive index of silicon nitride compared with silicon, which prevents easy coupling of light from the III-V material into the silicon nitride waveguides.

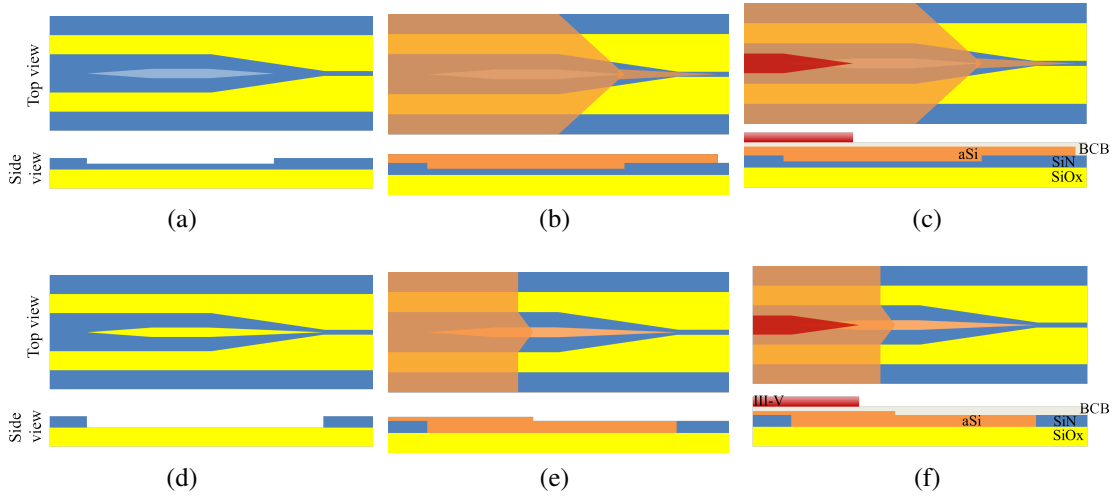


Figure 1: Two spotsizer designs to couple light from the III-V into the silicon nitride waveguide: (a-b-c) shallowly etched taper, (d-e-f) fully etched taper. (red: III-V, grey: BCB, orange: amorphous silicon, blue: silicon nitride, yellow: silicon oxide)

In this paper we present a new coupling approach from III-V to silicon nitride, based on a spotsizer that uses amorphous silicon as an intermediate coupling layer. Since the proposed method can be done completely in silicon, we can leverage from the supreme fabrication technology inherent to silicon. According to simulations, this new technique can get to the standard of state-of-the-art III-V to silicon spotsizer converters.

Two taper designs

We will look at two different spotsizer designs, depicted in figure 1. Because the refractive index of Si_3N_4 is too low, we cannot achieve phase matching between the silicon nitride waveguide and the III-V mode, so no light will couple from the III-V to the silicon nitride. In order to solve this problem, we will first couple from the III-V to an intermediate amorphous silicon (aSi) layer and only then the light will be coupled to the silicon nitride waveguide.

To make the III-V–aSi spotsizer, first a taper is etched in the middle of a broad silicon nitride waveguide. This happens in the same etch step as the silicon nitride waveguide definition and is therefore self-aligned. In the first design, only part of the silicon nitride is etched as is shown in figure 1a. In the second design, the silicon nitride is fully etched as shown in 1d.

Next the chip is covered with aSi. The taper etched in the silicon nitride waveguide is now filled with amorphous silicon. Furthermore, the aSi is patterned in order to couple the light from the aSi to the Si_3N_4 . The amorphous silicon needs to be thick enough to allow for easy coupling between the III-V and the silicon. This means that the aSi layer on top of the silicon nitride waveguide will be thicker for the case of the shallowly etched taper (figure 1b) than for the fully etched taper (figure 1e).

To couple the light in the Si_3N_4 waveguide, two approaches are considered. When the taper is fully etched, only a thin layer of aSi is present on top of the Si_3N_4 waveguide. First, a taper with a broad taper tip is used to couple the light completely in the etched

taper. Next, the etched taper couples to the silicon nitride waveguide, as illustrated in figure 1e. On the other hand, in figure 1b the light will first couple from the etched taper into the aSi waveguide on top of the silicon nitride. Subsequently, the aSi waveguide will taper down to couple the light in the Si_3N_4 waveguide. Because all this can be done before bonding, no complex post-processing is necessary.

Finally, the active material is bonded onto the silicon nitride chip and an adiabatic taper is formed in the same way as on the SOI platform [4]. This means that no power exchange occurs between the fundamental waveguide mode and the higher order waveguide modes. This is shown in figures 1c and 1f.

Simulation results

In order to evaluate the working of the two taper designs, simulations were carried out with FIMMWAVE, a commercial eigenmode solver (by Photon Design). We assumed a silicon nitride waveguide thickness of 300 nm and a shallow etch step of 150 nm. The simulation results shown here are all for a wavelength of 1550 nm, but we can see the same trends when using 1310 nm light.

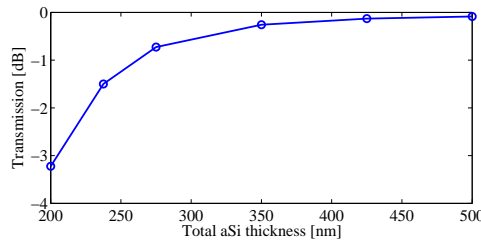
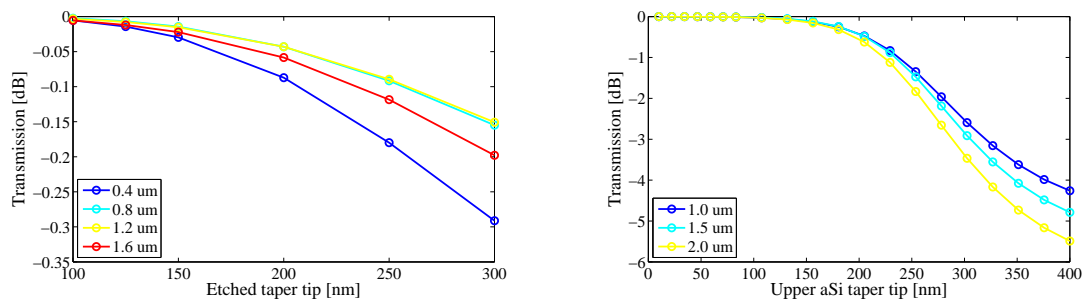


Figure 2: Transmission from the III-V mode to the amorphous silicon as a function of total aSi thickness.

In figure 2 one can see that a minimal amorphous silicon thickness is needed for good coupling from the III-V mode into the silicon taper. We assumed a III-V taper tip width of 500 nm and a BCB thickness of 50 nm. For the simulations a layerstack similar as in [4] is used.

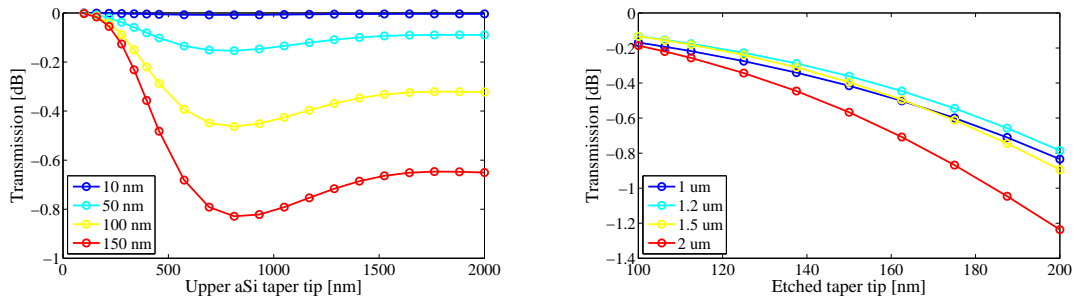
A narrow upper amorphous silicon taper tip is of key importance for good coupling between the aSi layer and the silicon nitride waveguide. Figure 3b shows this coupling as



(a) Coupling from the etched taper to the upper aSi waveguide as a function of etched taper tip for different upper-waveguide widths. (b) Coupling from the aSi into the silicon nitride waveguide as a function of aSi taper tip for different Si_3N_4 waveguide widths.

Figure 3: Simulation of the shallowly etched taper.

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(a) Coupling from the upper aSi into the etched aSi taper as a function of upper aSi taper tip for different aSi upper layer heights. (b) Coupling from the etched taper to the silicon nitride waveguide as a function of etched taper tip for different Si₃N₄ waveguide widths.

Figure 4: Simulation of the fully etched taper.

a function of aSi taper tip width. Less crucial is the width of the etched aSi taper, as is shown in 3a. For these simulations we assumed a aSi thickness of 150 nm + 250 nm. In figure 4 the transmission characteristics of the fully etched taper design are plotted as a function of taper dimensions. The width of the etched aSi taper is 2 μm. The thinner the aSi layer on top of the silicon nitride, the less sensitive the coupling is to the tip width of the upper taper, as shown in figure 4a. Figure 4b shows the importance of a narrow etched taper to allow for good coupling between the aSi and the Si₃N₄ waveguide. In the shallow etched technique the taper transmission is most sensitive to the width of the upper taper tip, where in case of the fully etched taper the width of the etched taper tip proves to be the most crucial. Depending on which process proves to be the least trivial, either approach can be used.

Conclusion

A promising new coupling technique is presented that allows for easy heterogeneous integration of III-V materials on the silicon-nitride-on-insulator platform. Two coupling approaches are evaluated. According to simulations, both techniques can get to the standard of state-of-the-art III-V to silicon spotsize converters.

References

- [1] F. Doany *et al.*, “Multichannel high-bandwidth coupling of ultradense silicon photonic waveguide array to standard-pitch fiber array,” *Lightwave Technology, Journal of*, vol. 29, no. 4, pp. 475–482, 2011.
- [2] B. Snyder *et al.*, “Hybrid integration of the wavelength-tunable laser with a silicon photonic integrated circuit,” *Journal of Lightwave Technology*, vol. 31, no. 24, pp. 3934–3942, 2013.
- [3] M. Heck *et al.*, “Hybrid silicon photonic integrated circuit technology,” *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 19, no. 4, 2013.
- [4] G. Roelkens *et al.*, “Iii-v-on-silicon photonic devices for optical communication and sensing,” in *Photonics*, vol. 2, pp. 969–1004, Multidisciplinary Digital Publishing Institute, 2015.
- [5] S. Kumari *et al.*, “Integration of gaas-based vcsel array on sin platform with hcg reflectors for wdm applications,” in *SPIE OPTO*, pp. 93720U–93720U, International Society for Optics and Photonics, 2015.