Fabrication of substrate-less planar silicon photonic crystal cavities

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Integrated free-standing planar silicon photonic membranes with a complete free access to each of their sides may offer interesting practical opportunities to develop advanced photonic sensors. One challenge is to remove the substrate without jeopardizing the photonic properties of the sensing area. Here, we present a reproducible process for the fabrication of substrate-less silicon photonic crystal cavities. With such a process, substrate-less windows as large as 1.2 mm x 60 µm can be opened, which allows us to access a large amount of sensor areas from both sides. We show that cavities with quality factors as high as 3000 are unaffected by the process.

Introduction

Suspended dielectric planar photonic crystal (PhC) cavities can combine high quality factor (Q) as high as 2 x 10^6 with effective mode volume (V_m) as low as 0.066µm^3 [1], which enables refractive index sensing with high sensitivity. For instance, the presence of biological molecules in the surrounding of the cavity can result in a frequence shift of the cavity resonance. Even if transportation of molecules to the sensing surface with different kinds of micro-fluidics channels have been implemented, in some case such approaches can be inefficient [2].

Here, we propose another solution to allow new detection schemes. By opening a micron size window below the PhC cavity, effective injection of analytes to the sensing area can be realized in much lower concentration (even down to single molecule level). In this paper, we introduce a very consistent process for fabrication of such suspended PhC cavity, which provides access to both side of sensing area without affecting the photonic properties. This kind of processed chip enables the simultaneous measurement of intensity fluctuations from the top surface of the cavity that comes from any dielectric perturbations at the bottom surface. Substrate-less photonic structures can also be realized by removal of silicon substrate before patterning of any photonic structure as reported in [3] or in [4]. However, it is currently only feasible for small opening windows of size 0.25 mm x 0.25 mm, which limits the number of devices that can be targeted.

Fabrication

Planar photonic crystal fabrication was performed using deep – UV lithography on SOI wafers which consist of a 220 nm top silicon layer on a 2-µm-thick buried silicon dioxide (BOX) layer, on top of a 725-µm-thick silicon substrate. After patterning the photonic structures, the wafer was diced in 2.5 cm x 2.5 cm individual chip. The chip was thinned and polished using a chemical mechanical polishing machine. The chip is thinned by mounting that on a vacuum chuck on which the substrate is pressed down against a rotating pad. Silica based chemical slurry is flown continuously over the pad to mechanically etch the substrate. In next step, silicon substrate has to be etched underneath the photonic structures of interest from thinned sample. For this purpose 500 nm of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) were deposited as hard mask on polished side of silicon substrate using plasma enhanced chemical vapour deposition (PECVD) technique. Any scratch on polished side of chip has to be avoided as it can lead to peeling of hard mask during silicon etching process.

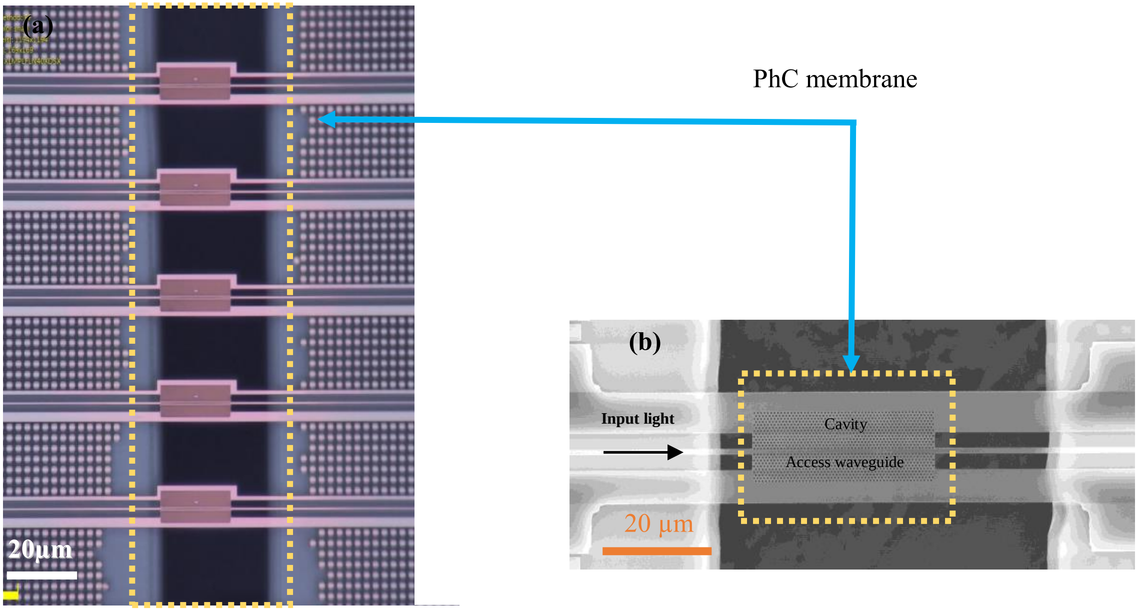

Figure 1: (a) Optical microscope image of substrate-less PhC membrane. (b) scanning electron microscope (SEM) image of PhC membrane (cavity is excited by input light coupled into access waveguide).

Using contact lithography in backside alignment mode a window was pattered through which silicon will be etched in potassium hydroxide (KOH). Since KOH etches silicon anisotropically, the patterned size of window was much bigger size on backside of silicon substrate than opening window of PhC cavity on the device layer. After contact lithography, hard mask was etched from the patterned window in reactive ion etching (RIE) followed by silicon etching in 20% KOH solution at 80 °C which etches silicon with 1.2µm/min. Here the 2-µm-thick buried silicon dioxide (BOX) acts as an etch stop layer. Once all the silicon has been etched, BOX was etched in 40% HF which etches silicon dioxide at rate of approximately 900nm/min followed by drying etched sample in Critical Point Dryer (CPD) to avoid stiction. SiO_2 etching in HF has to be monitored carefully as excessive etching will lead to huge undercut which in turn collapses membrane. Figure 1(a) shows optical microscopic image of fabricated window of substrate-less PhC membrane from above described process and Figure 1(b) shows scanning electron microscope (SEM) image of one such PhC suspended membrane. This process to fabricate substrate-less membrane can be used for other structures as well such as gratings, waveguides, ring resonators etc.

Measurements

Figure 2(a) shows a schematic of the experimental apparatus used for PhC characterization. It highlights the opening of the sample at the bottom and the local light collection at the other side. The photonic crystal structure is excited by a tunable laser diode at 1.55 µm (Tunics) through a polarization controller, which can excite TE or TM mode separately. The polarized light is then injected into the processed sample via lensed fiber and access waveguide.

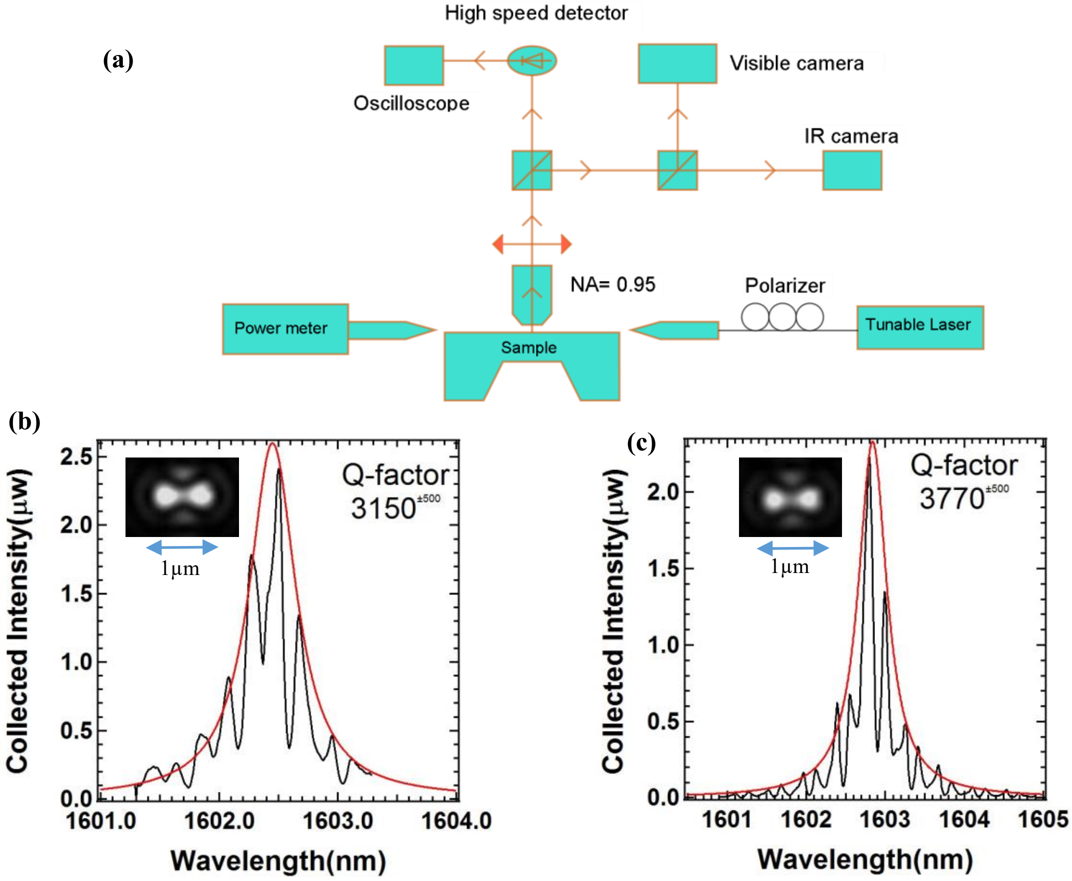

Figure 2. (a) Schematic of the experimental apparatus used for PhC characterization. (b), (c) transmission spectra of substrate-less PhC cavity and cavity without substrate removal respectively. (Inset- intensity pattern of the cavity field at resonance)

The light radiating out of the cavity surface is collected through a high numerical aperture (0.95) microscope objective and directed toward an infrared camera and InGaAs photodetector. Standard L3 defect in a PhC is created by removing 3 holes along Γ-K direction which has quality factor of approximately 3000 [5].

The cavities were excited through a W1 waveguide (line defect waveguide constructed by removing a row of air holes) separated by 4 rows of holes from the cavity. Figure 2(b) and 2(c) shows transmission spectrum (black line) together with Lorentzian fit (red line) of respectively underetched (local BOX removal) but without substrate removal and backside etched (substrate-less without any BOX) L3 cavity collected from cavity surface.

The oscillation in transmission spectra of cavity is due to strong Fabry-Perot interference caused by reflections at the sample facets. Inset of Figure 2(b) and 2(c) shows intensity pattern of L3 cavity with lattice constant, a = 440 nm and hole radius, r = 105 nm. We can infer from these graphs that the quality factor extracted by Lorentzian fit of transmission spectra and mode of substrate-less L3 cavity is similar to that of cavity of which only local BOX was etched.

Conclusion

We have developed a reliable method to fabricate substrate-less PhC membranes. As the process does not jeopardies the photonic properties of the devices, these devices can be used for analyte sensing with lower analyte volume.

References

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