Wet Etched Silicon Interposer for the Connection of CMOS ICs and Optoelectronic Dies

C. Li [1], E. Smalbrugge [1], R. Stabile [1] and O. Raz [1]
[1] COBRA Institute & Dept. of Electrical Engineering, Eindhoven University of Technology, the Netherlands

In this paper, a novel wet etched silicon interposer for optical interconnection applications has been proposed and fabricated. The interposer concept is conceived to include, via flip chip bonding, both CMOS ICs and optoelectronic dies to allow close proximity of electronics (drivers, TIAs) to photonics (VCSELs, PDs). The fabrication steps are developed to realize silicon recessed areas, to fit the semi-conductor circuitry, and openings to fit mechanical optical interface (MOI). Two steps of silicon anisotropic wet etch are performed to define these areas. The metal traces for electrical connection are designed to match the impedance for signal transmission and are lithographically defined. The obtained silicon interposer is shown and the process challenges discussed.

Introduction

In the past few decades, the performance of data centres (DC) and High-performance computing (HPC) has been growing with an exponential rate [1]. To sustain this growth rate, it is projected that existing electrical interconnects in standard 19" width rack equipment connecting ASIC and pluggable transceivers on the front panel will be replaced by mid-board-optics (MBO) due to the front panel bandwidth density limits [2]. The footprint and the cost of the key modules (transmitter and receiver) are the main limitations, mostly due to the complex packaging. At present, the vertical-cavity surface-emitting lasers (VCSELs) and surface normal photodetectors (PDs) arrays are the most promising photonic technology to realize transceivers. During the fabrication, the components are packaged on printed circuit boards (PCB), where dense integration is complicated and costly to assemble and fabricate. Besides, point-to-point wire bonding is employed to make the connections between the CMOS IC and optoelectronic dies, which increases the cost and suffers from limited RF performance [3].

Silicon is the preferred carrier to be used for packaging, because mature CMOS technology can be utilized. It provides a robust, reproducible and low-cost solution. In addition, silicon as interposer material has a coefficient of thermal expansion (CTE) similar to the dies used in the assembly, which prevents thermal related stress associated to the CTE mismatch [4]. Also, the way to fabricate the silicon interposer plays an important role in defining transceiver cost. Wet etching of silicon is preferred to dry etching since it is a standard low cost process, and double-side wet etching has been proposed to realize the electrical through silicon via (TSV) [5] which has played a key role in the progress towards 3D stacked ICs.

In this paper, we take advantages of silicon wafer scale process, and fabricate a novel silicon interposer by wet etching and double side-etching. The patterned silicon interposer is then gold plated to link the dense interconnections between the FR-4 PCB and the silicon ICs. Also, funnel-shaped TSV are realized to couple the laser light from a VCSEL to the mechanical optical interface (MOI) and Multiple-Fiber Push-On/Pull-off (MTP/MPO) connector.

Scheme of the assembly

We propose a scheme to assemble the components scalable to wafer level packaging/assembly, which can provide the high performance and cheap transmitter module. As shown in Fig.1, the silicon interposer has been designed to assemble the CMOS driver, VCSEL and MOI. The chips, VCSELs and driver, are embedded in the silicon interposer. Lithographically defined metal traces, impedance matched for high speed transmission, are defined at the front-side of the interposer. At the backside of the same interposer the MOI are placed after opening the squared TSV to get light from the 12 VCSEL channel.

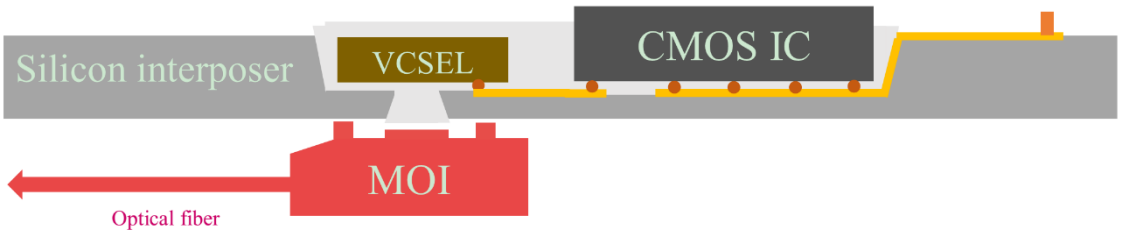

Fig.1 scheme of assembly CMOS driver, VCSEL, MOI

Only three low resolution lithographic steps are needed to pattern the silicon interposer, and both the front and the back side of the silicon interposer are utilized for electrical and optical connection, respectively.

Fabrication process

The proof-of-principal process is performed on a 1 inch double side polished silicon wafer, with (100) orientation and 280 µm thickness. Three hundred nanometers thick silicon nitride (SiN_x) is deposited on both sides of silicon (Fig.2a), after that the 1st wet etching takes place and a thin layer of silicon is left at the bottom of the recessed area (Fig.2b). After sputtering the gold seed layer, a 2nd lithography step is carried out on the 3D profile for subsequent metal electro-plating. (Fig.2c). Finally, a 2nd wet etching is made to open the optical TSV (Fig.2d).

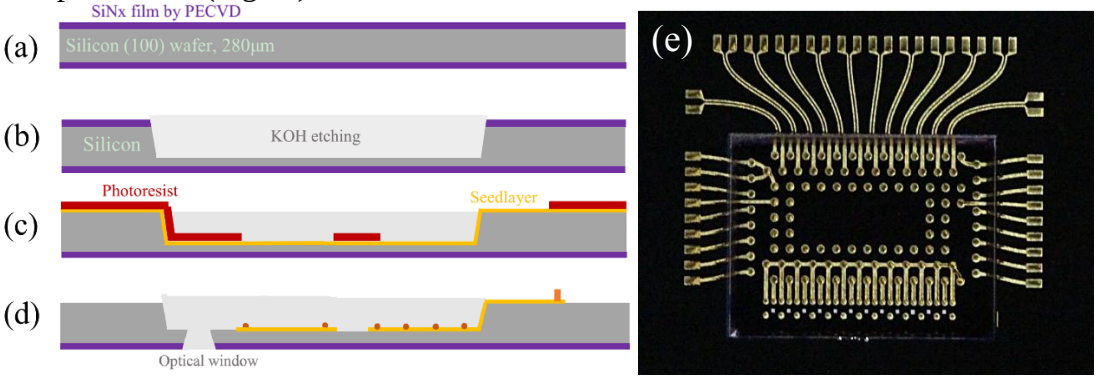

Fig. 2 process flow of silicon interposer (a) PECVD on both side; (b) KOH etching; (c) lithography on 3D structure; (d) chemically etching metal traces and 2nd KOH etching (e) finished silicon interposer.

For the 1st lithography step the edge of pattern is aligned to be in parallel to the <110> direction. The ma-N 440 photoresist is used for defining a large rectangular area. After dry etching of the SiN_x, a 35% (by weight) KOH (potassium hydroxide) solution is used for anisotropic etch of the silicon wafer at 80℃ for 200 minutes, and the SiN_x acts as a

hard mask, protecting the covered areas. Large rectangular recessed areas with 54.7° slope sidewall are obtained since the etching rate for the <111> direction is hundreds of times slower than that in the <100> and other directions (see the schematic cross section in Fig.3a). The 230 μm deep recessed areas (see Fig. 3b) is used to place the CMOS ICs and optical dies. However, this sidewall shape is not ideal for spin coating, because the photoresist cannot easily cover the steep corners. Therefore, an additional Tetramethylammonium hydroxide (TMAH) etching is performed to smooth the corners [6]: the faster etching rate along the crystal directions between <100> and <111> results in smoother corners. After 25 minutes etching in 20% (by weight) TMAH solution at 80℃, a round corner is obtained (see cross section in Fig.3c).

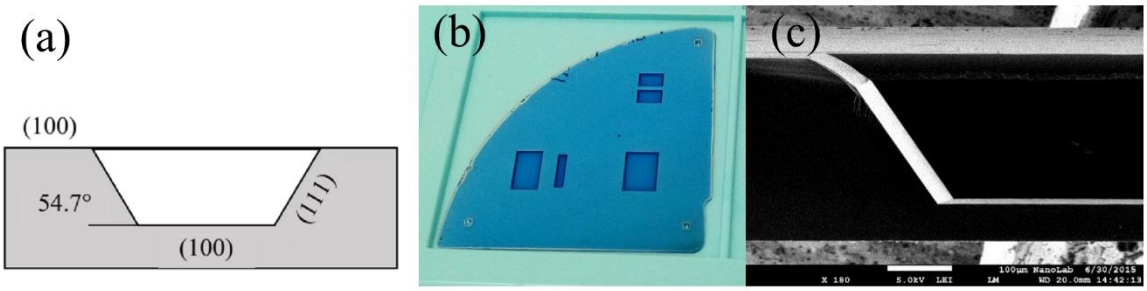

Fig. 3 (a) scheme of anisotropic wet etched profile of (100) silicon; (b) photo of 1 inch silicon wafer with etched holes, with a passive layer of SiN_x; (c) SEM photo of cross section of etched wafer, with smoothed corner and the side wall

The 2nd lithography is carried out on the already etched structure, after sputtering the seed layer for plating. The thick positive chemically amplified photoresist AZ® 40XT is employed for electro-plating. As shown in the Fig. 4(a), the photoresist is smoothly continuous after exposure and development of the photoresist: the light traces are the opening in the photoresist. A one micron thick layer of gold is then plated. Fig. 4b & c, shows the fan-out differential traces and short ground signal ground (GSG) traces between CMOS and VCSEL array after removing the seed layer.

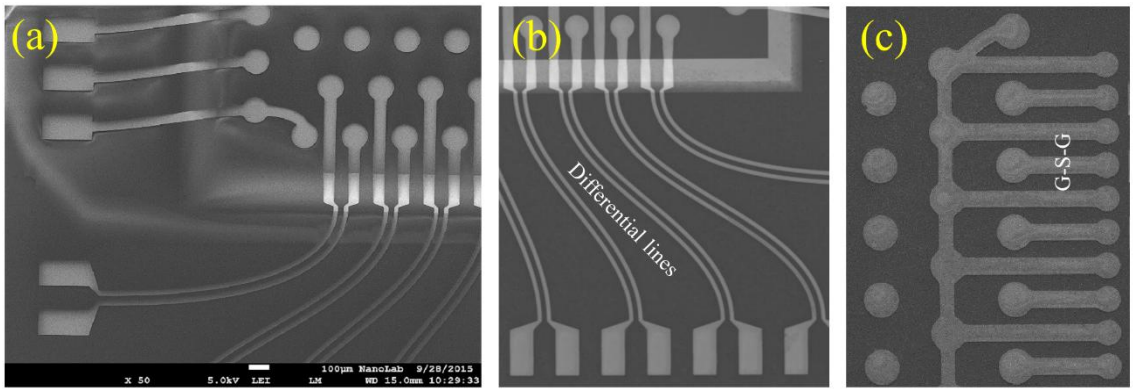

Fig. 4 (a) lithography on 3D structure; plated gold traces for defining the differential lines. Plated differential lines (b) and GSG lines (c).

In order to make the funnel-shape TSV for light coupling, the last step of lithography is carried out on the backside using the same KOH wet etching process used on the front side. After 50 minutes, the remaining thin layer of silicon is etched through, and the optical windows are created (see Fig. 5a). The backside SEM photo (Fig.5c) shows the

active region of VCSELs and the funnel-shaped optical windows, which will help to confine the light. The finished silicon interposer is shown in Fig.2e, and it is now ready to start the assembly of the optoelectronic and CMOS dies. A FINEPLACER® lambda die Bonder was employed to align the two chips. Firstly, we use gold-gold metal bonding between the pads on VCSEL and silicon interposer, with the thermal (300℃, 30s) compression (1N/pad) method. After that, the CMOS driver, with solder bumps on it, is placed and reflowed using the die bonder. The final assembled sample is shown in Fig.5b.

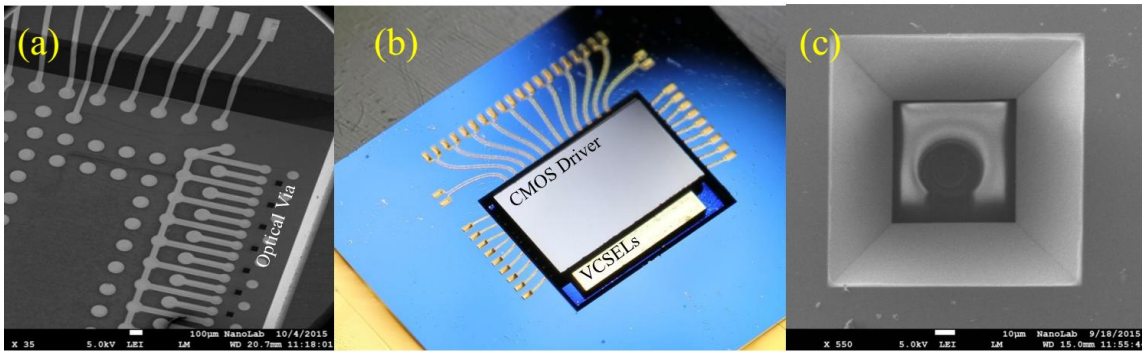

Fig. 5 (a) photography of silicon interposer (b) photo of assembled silicon interposer (c) one of 12 optical windows, opened form the backside, and active region of VCSEL.

Conclusion

In this paper, we demonstrated a new wafer level approach for optoelectronic packaging. We introduce the silicon interposer to connect the CMOS IC and optoelectronic dies, and make use of the both sides of the silicon interposer. One side is used for electrical connection, and the other side is used for optical connection, achieved by optical TSV.

In the future, the MOI will be mounted on the transmitter module, and the performances of the transmitter module can be tested. Further, the new processes for making the silicon interposer will be repeated on a thicker wafer, and deeper recessed area will be made to fully embed the CMOS chip. Thus, the optical engine will be more flexible and can be flipped on any carrier.

Acknowledgements

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