Design of a segmented modulator driver for advanced modulation formats

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This paper presents the requirements, design trade-offs and technology options for segmented modulator driver circuits. The electronics design of such drivers is very different from conventional Mach-Zehnder modulator driver designs. Thanks to the segmentation of the relatively long traveling wave electrode, a significant amount of power can be saved by avoiding the traditional 50 Ohm interface. Instead, a segmented modulator driver drives multiple small lumped capacitive loads. Moreover, the novel transmitter structure allows for the creation of multi-level optical signals without the use of DACs and linear drivers, enabling direct digital drive with low voltage swings from a deep submicron CMOS technology. However, the segmentation brings new challenges for the electronics, especially the timing, skew and mismatch between the different drive signals, which require special attention to electro-optical co-design to preserve the optical signal quality.

Introduction

Scaling next-generation optical networks to higher capacities will require architectures with higher spectralefficiencies to optimally use the available bandwidth. The use of advanced modulation formats allows for higher data rates without increasing the clock rate and hence avoids excessive impairments induced by the optical channel. Moreover, tight channel spacing in DWDM is still possible due to the narrower spectrum. These advanced modulations pose severe challenges for the transmitter and receiver electronics due to the need for high-speed multi-level signalling while at the same time maintaining a power efficient and cost-effective solution. A promising solution for the generation of advanced multi-level signals is a sequentially-driven segmented Mach-Zehnder modulator (MZM). Co-designing the driver with the modulator is crucial to achieve optimal performance.

Segmented modulator-driver configuration

In current state-of-the art MZ modulators, an electrical signal drives a travelling-wave (TW) electrode in a push-pull configuration, resulting in a phase shift in each of the arms of the modulator. Combining the two optical paths gives rise to amplitude modulation due to interference. The main electro-optic bandwidth limitations in travelling-wave modulators are the velocity mismatch between the electrical and optical signal on the one hand and microwave losses on the electrode on the other hand. The modulation efficiency is determined by the $V_\pi L$ (half-wave voltage x interaction length) constant of the technology imposing a strong trade-off between driving voltage and bandwidth. The segmented structure as shown in Figure 1 is an innovative way to overcome this trade-off [1].

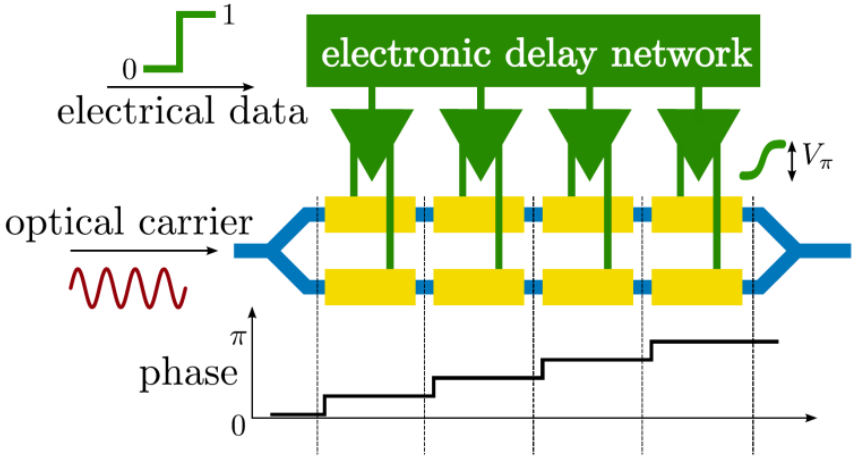

Figure 1: Working principle of the segmented architecture

In this approach, a driver array sequentially applies a data signal to a series of electrode segment pairs. Instead of a continuous increase of the phase shift on a travelling-wave electrode, the electrode is split in a number of segments to change the phase in a discrete way. The delay of the optical path in between two segments is matched by a timing circuit in the electronics. Due to the delay-separated drivers, the total interaction length of the modulator can be increased without suffering from velocity mismatch or microwave losses. As a result of this elongation, the effective V_π can be as low as $1\,V$ [2], allowing the use of low-power driver electronics. A single segment is considered to be sufficiently short to be treated as a lumped, mainly capacitive, impedance. This avoids the use of a transmission line interface with a $50\,\Omega$ termination, providing another opportunity for a gain in power efficiency.
Advanced optical modulation formats are commonly generated by driving the TW electrode with multi-level electrical signals using an electrical high-speed DAC, followed by a linear driver. In the proposed transmitter architecture, the effective interaction length is varied, rather than change the drive voltage by using power-hungry components. By altering the number of segments contributing to the modulation, different optical signal levels can be generated with only binary drive signals. QAM-constellations can then be created by nesting two MZMs in an IQ-configuration. For an IQ-transmitter, the two MZMs are commonly biased at its zero-transmission point and a differential drive voltage of $2 * V_\pi$ is required in order to reach all 4 quadrants of the constellation diagram. Recently, DAC-free 16-QAM generation has been demonstrated with a segmented structure [3]. Furthermore, the efficient DAC functionality also enables transmitter-side DSP such as filtering and linearization [4].

Design choices and challenges

Because there is no need for a $50\,\Omega$ interface, nor for a linear driver, there is additional freedom in choosing a proper driver topology. Table 1 depicts the basic schemes of two possible driver topologies: a current mode logic (CML) driver consisting of a differential pair and a CMOS inverter chain, to be used in a pseudo-differential chain. Since a segment can be considered to be a lumped capacitive load, the static power consumption of an inverter chain is negligible in contrast to the CML topology. Within a technology node, the CMOS inverter delivers the highest swing as it switches from ground to supply. Though this swing is fixed, it can be matched to the modulator by choosing a proper interaction length. As the segmented configuration can reduce the

effective V_π voltage down to $1\,V$, a CMOS inverter topology in a deep-submicron technology appears to be an ideal candidate to implement a power-efficient solution.

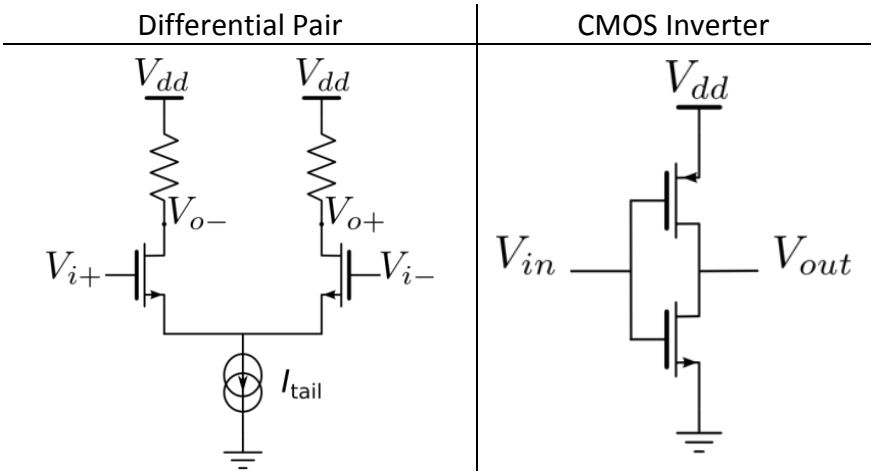

Table 1: The differential pair and the inverter as possible driver topologies

However, caution has to be taken in applying the proper drive signals to the segments with this topology. The key difference between both drive schemes is that the drive voltages are not symmetric around zero for the inverter drivers since it is a pseudo-differential solution. When considering the transfer function of an MZM, in which V_1 and V_2 are the sum of the different segment voltage contributions applied to the two arms of the MZM (shown in Figure 2), one can see that the difference between the voltages controls the amplitude of the optical signal, while the sum of the voltages determines the phase of the output:

$$\mathrm{H_{MZM}} = \mathrm{E_{out}/E_{in}} = \exp\left(j\frac{\pi}{2V_\pi}(V_1+V_2)\right)\cos\left(\frac{\pi}{2V_\pi}(V_1-V_2)\right)$$

When using the CMOS inverter, the sum of the voltages differs when altering the numbers of segments contributing to the modulation, resulting in an undesired phase shift. As a solution, a configuration is proposed which combines positive and negative polarities of segment pairs to alter the amplitude, hence keeping $V_1 + V_2$ constant. The length of the last segment is hereby halved to provide the same resolution as the initial configuration. An example drive state is shown in Figure 2. V_1 gets a contribution from 2.5 segments and V_2 from 1 segment, so there is a net differential contribution of 1.5 segments.

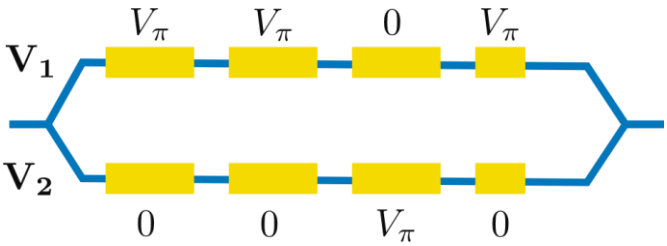

Figure 2: Drive state for multilevel generation with inverter drivers

Another important design parameter is the choice of the number of segments and the relative lengths (ignoring the half-length segment here for clarity). The segment configuration directly determines the resolution of the DAC functionality. As in

traditional DAC architectures, the two main candidates are a topology with all-equal segments and a binary weighted topology. The former allows for a more straightforward driver design since all output channels see the same load. However, the number of segments needed, grows exponentially with the desired resolution of the output signal, resulting in excessive power consumption and difficulties in integrating the electronic and optical chip. On the other hand, a binary weighted solution results in a minimum number of segments. The drawback is that the large difference between the loadsbecomes impractical for the electronics. In practice, a hybrid solution combining the two approaches, will yield the most efficient implementation for a sufficiently high resolution.

The main challenge for the electronics is to provide the different driving signals with an accurate timing. A first potential source for errors is timing skew in the two driving voltages for a single segment pair. This is only an issue when using CMOS inverter chains since the signal is not inherently differential. The timing mismatch can be alleviated by cross-coupling the two chains, posing a trade-off between bandwidth and timing skew. A second source of mismatch occurs when the velocity of the optical signal is not exactly matched in the electronics. The delay between two channels is typically in the order of picoseconds, therefore requiring very precise timing circuitry. Moreover, the exact value of the inter-segment delay can vary due to process variations during fabrication of the MZM. Though the value is constant for a single MZM, the mismatch with the driver accumulates during the propagation over the interaction length. As a consequence, it is crucial to have tunable delay cells with a precise value and at the same time feature a large tuning range. A last source of timing errors is introduced by mismatches between the different channels. On the one hand by process variations in the electronics fabrication and on the other hand the load capacitance can be different due the choice for unequal length segments. These delay errors do not accumulate, hence the use of a second set of delay cells is recommended.

Conclusions

A periodically-driven segmented MZM is considered, capable of generating advanced modulation formats using only digital drive signals. Additional complexity is shifted to the electronics, where multiple drive signals have to be delivered with accurate timing. Low-power CMOS inverters in a deep-submicron technology appear to be an interesting driver topology.

Acknowledgements

This work was supported by the European Commission through FP7 project SPIRIT and by the Agency for Innovation by Science and Technology in Flanders (IWT).

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