48×10 Gbps Cost-effective FPC Based On-board Optical Receiver with Commercial PGA Connector

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We report a flexible printed circuit (FPC) based 48 × 10 Gbps on-board optical receiver. Compared to currently commercially available modules such as QSFP+, SFP+, our low-cost receiver module, 3.15 cm x 3.15 cm sized containing 48 channels, can offer smaller footprint and larger bandwidth density to overcome the limitation of front panel bandwidth. Error free performance at 10 Gbps can be achieved for all 48 channels and eye-diagrams for selected channel are shown.

Introduction

Future data center networks (DCN) must support more bandwidth and consume less power per bit. Optical transceiver modules should be improved to follow the performance development of the DCN [1]. Current commercially available switches are using pluggable front panel transceiver. These pluggable transceiver modules are always overcrowded into the front panel of the switch box for ease of accessibility resulting in long transmission lines connecting them to the switch ASIC. These factors limit the eventual total bandwidth and make the whole system more power hungry [2]. Compared to pluggable optics, on-board optics is a promising solution to overcome the front panel bandwidth limitation and can also reduce power consumption by making on-board re-timers redundant. In order to achieve optical modules with high channel counts, expensive and complicated packaging technology is often used [3].

We have recently demonstrated a low-cost FPC based 48×10 Gbps on-board optical transmitter [4]. In this paper, we present a FPC based 48×10 Gbps on-board optical receiver. This compact on-board receiver is only 3.15cm × 3.15cm, and contains 48 channels operating at 10 Gbps. In order to ensure easy and low-cost packaging we use direct die attach approach for our assembly. Thermal solder reflow making use of a specially designed hotplate is used to attach the TIA chips and ultrasonic bonding process is applied on PDs to FPC by using a flip-chip machine. Optical straight lens connectors are used to couple the light to a single 48 fibers MT connector. To verify the high-speed performance, the fully assembled receiver is tested at 10Gbps. Bit error rates as well as eye diagrams at 10Gbps for representative channels are reported.

FPC Design

A schematic drawing of the FPC based receiver is shown in Fig. 1(a). The FPC is used as the base material in this module, due to the good high-speed performance and low-cost. This FPC is based on a low loss polyimide material (dielectric constant of 3.2 and a dissipation factor of 0.002 at 1 MHz) with 2 copper layers sandwiching a thin insulating polymer film. Conductive circuit patterns are affixed on both sides of the polymer layer to allow interconnections between TIAs and connection to the ISI PGA. A second thin polymer coating is typically supplied to protect the metal tracks. In the center of the FPC, 50μm wide coplanar differential pairs for 4 separate 12-channel

receivers are routed. Along the edge of the FPC, 1mm pitch round pads for a PGA connector are located. A commercial ISI HoLi 556 PGA connector is machined to have a hole in the middle to leave space for the electronic and optical components. The ISI PGA connector itself has been shown to support 20 Gbps signaling [5]. The paths used for sending digital high speed signals within the FPC go from the PGA pads to the TIA chips. The frequency response of the differential transmission lines on FPC is obtained using Polar SI9000, and their characteristic impedance is calculated and optimized to be 100Ω. The impedance matched differential pair have 50µm width and 50µm gap (between two differential pairs) and 150µm gap from the ground plane. The drawing of the FPC layer stack for a differential pair is shown in Fig. 1(b).

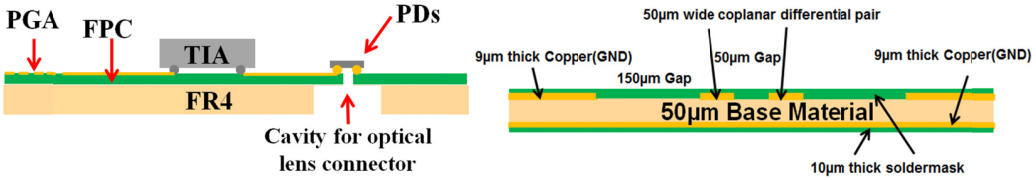


Fig. 1 (a) Schematic design of the on-board receiver; (b) Drawing for the cross-section of layer stack where the differential traces are.

Since the photo-detector is capacitive and the impedances of pads on the TIA differ largely from channel to channel, the connection between the photo-detector and the TIA should not be laid out as a transmission line above a grounded substrate. A tight coupling between the anode and cathode connections is desirable to reduce lane-to-lane crosstalk as these carry equal but opposite RF currents. As a result, the photo-detectors are put close to the TIA chips, at a distance of only 300 µm.

Packaging Process

The top view of the fabricated FPC is shown in Fig. 2. A 440µm thick FR4 stiffener is glued at the back of FPC to improve the stiffness of the FPC. The thermal expansion coefficient of the stiffener is close to the thermal expansion coefficient of the FPC, which avoids possible CTE mismatch related issues during the high temperature reflow processes. Four cavities have been designed in this FR4 layer to allow the insertion of optical connectors.

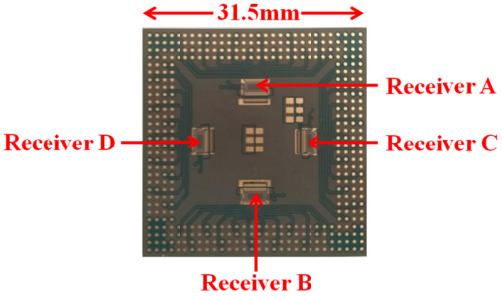


Fig. 2 Top view of the fabricated FPC

The FINEPLACER® lambda is used to flip-chip bond and ultrasonic bond both the TIAs and PDs through SnAg solder bumps reflow and gold-gold connection. Ultrasonic bonding process is applied between the PD array and FPC. Gold stud bumps are used as a fixed spacer to avoid short circuits during the reflow process. To further improve the stiffness of the FPC substrate during the die reflow the hotplate has been machined with a relief for holding the FPC in the cavity during the bonding. When using a standard flat hotplate, the air inside the cavity has a much lower thermal conductivity, reducing the

heat transfer from the hotplate to the pads on FPC and solder bumps on chips. The specially designed hotplate is made of aluminum, which has a high thermal conductivity greatly improving to heat transfer between the hotplate and the pads on the FPC. After the solder reflow and ultrasonic bonding process, optical straight lens connectors with size of 2.6mm × 6.4mm are glued through the cavities with epoxy. Each connector contains 12 optical lenses in parallel with a pitch of 250 µm, matching that of the PD array. The FINEPLACER® Lambda is also used to align the lenses to the PDs. The packaging processes are shown in Fig.3.

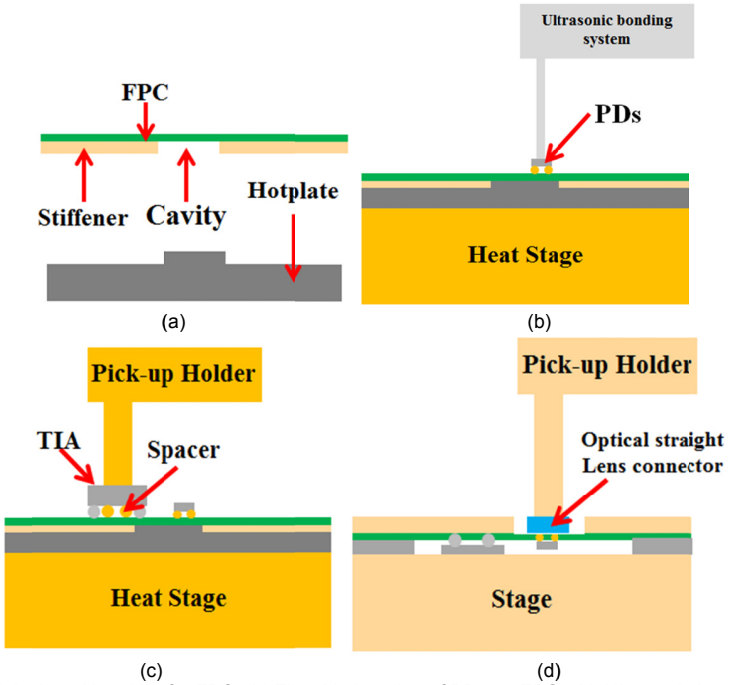


Fig. 3 (a)Special designed hotplate for FPC; (b) Flip-chip bonding of PDs on FPC with Ultrasonic bonding process; (c) Flip-chip bonding of TIAs on FPC with solder reflow process; (d) Assembly of the optical straight lens connectors to the module

The fully assembled 480 Gbps on-board receiver is shown in Fig. 4.

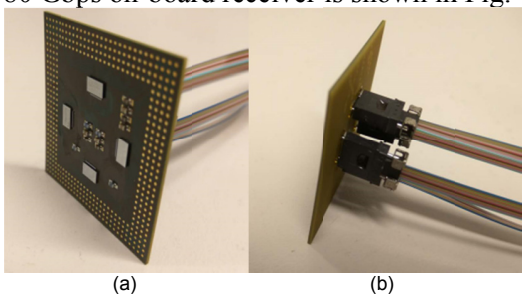


Fig. 4 4 × 12-channel MT fiber array ribbons connected to the on-board receiver: (a) front and (b) back side.

Experimental Results

The test set-up used to validate the performance of the 48 channel receiver module is shown in Fig. 5. A 10 Gbps differential electronic signal generator with 2^{31} –1 non-return-to-zero (NRZ) pseudo random binary sequences (PRBS) is injected into an SFP+ module to generate the optical signal. The signal is then input through the fiber array through the four optical straight lens connectors, which are mounted on the top of FPC,

then transferred into PDs. After photo detection takes place in the PDs, the signal is amplified by the TIA chips, and sent to the error detector through a 1mm pitch RF differential probe.

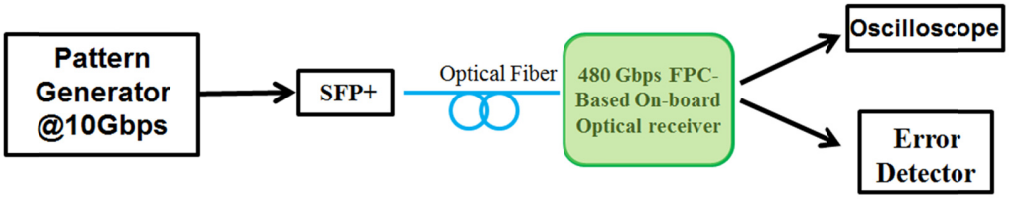
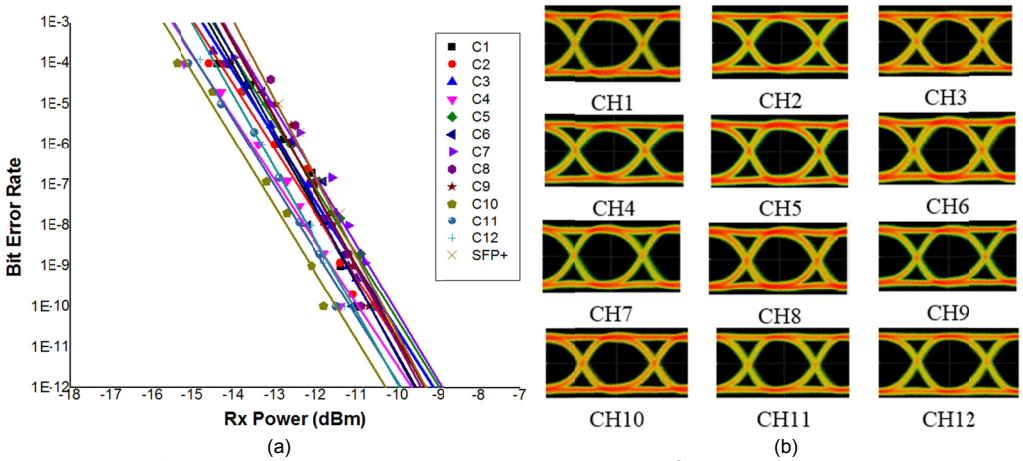


Fig. 5 Experimental set-up

All 48 receiver channels show error free performance at 10Gbps. The eye-diagrams and bit error rate (BER) of selective channels are shown in Fig. 6.



(a) (b)

Fig. 6 (a) Bit error rate (BER) curves and (b) eye-diagrams for selective channels.

Conclusion

In this paper, we propose a FPC based on-board optical receiver, which is only 3.15cm × 3.15cm, and contains 48 channels. The low-cost packaging approach of this module uses direct die attach principle employing thermal solder reflow and ultrasonic bonding to mount the components on the FPC using a flip-chip machine without using any additional interposer. All 48 channels of the receiver show error free performance at 10Gbps and all eye diagrams are clearly open.

Acknowledgement

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