

A novel polishing stop for accurate integration of potassium yttrium double tungstate on a silicon dioxide platform

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Rare-earth ion doped potassium yttrium double tungstate, RE:KY(WO₄)₂, is a promising candidate for the realization of on-chip lasers and amplifiers. Two major bottlenecks difficult the realization of compact, high-contrast devices. Firstly, the crystal can only be grown on a lattice matched substrate, leading to a low ($\sim 10^{-2}$) contrast between core and cladding. Secondly, the required thickness for the high contrast waveguides, $\sim 1 \mu\text{m}$, makes the polishing step very challenging. In this work we propose a novel polishing stop that will permit to accurately control the final thickness of the KY(WO₄)₂ waveguide within a few hundreds of nanometers.

Introduction

Rare-earth ion doped potassium yttrium double tungstate, RE:KY(WO₄)₂ is a promising material for on-chip lasers and amplifiers. The high emission and absorption cross-sections, the large inter-ionic spacing and the high refractive index ($n \approx 2.00$ at $\lambda = 1.5 \mu\text{m}$) permitting the realization of compact waveguides makes efficient pumping without quenching possible.

Earlier work on rare-earth ion doped RE:KY(WO₄)₂ channel based waveguides was based on the growth by liquid phase epitaxy (LPE) of doped layers onto undoped substrates. Using this approach, amplifiers with a modal gain of $\sim 1000 \text{ dB/cm}$ at a wavelength of 980 nm [1], lasers with large tuning bandwidth [2] and high-power efficiency [3] have been demonstrated.

The aforementioned technology, however, has some disadvantages. Firstly, the refractive index contrast between the doped and undoped layer is low ($\Delta n < 2 \cdot 10^{-2}$ [4]), which leads to large footprint and modal cross-section, increasing the requirement for pump power to fully invert the gain material. Secondly, lattice matching is required in order to grow a defect free crystalline layer. This method is therefore not suitable for the integration of RE:KY(WO₄)₂ with dielectrics (i.e. SiO₂, Si₃N₄) or semiconductors (i.e., Si, InP).

High refractive index contrast waveguides are needed for applications where compact footprint and tight waveguide bends are required. High contrast waveguides require the integration of KY(WO₄)₂ onto low refractive index substrates such as SiO₂, which can be realized by means of heterogeneous integration. Firstly, the KY(WO₄)₂ sample is bonded to an SiO₂ substrate. After that, thinning to the required thickness is done by a combination of lapping and polishing. Sefunç et al. [6] demonstrated for the first time heterogeneous integrated KY(WO₄)₂ rib waveguides. In that work, a 2.4 μm thick KY(WO₄)₂ layer was transferred and subsequently patterned using focused ion beam (FIB) milling. However, the control of the final thickness is the bottleneck of this process, making it very difficult to achieve the 10's of nanometers of precision required for the final application.

In earlier work [7] we demonstrated the working principle of a novel integrated polishing stop to obtain thin RE:KY(WO₄)₂ layers. Namely, the KY(WO₄)₂ sample was bonded on

a pool etched on the SiO₂ substrate. When the KY(WO₄)₂ sample is polished till the surface of the SiO₂ substrate, the polishing speed drops by a factor of circa 4x, increasing the tolerance of the process. The final thickness of the thin KY(WO₄)₂ layer is then determined by the difference between the depth of the pool and the thickness of the bonding layer. However, the planarity of the layer stack plays a crucial role on the controllability of the thickness of the final layer. In this work we demonstrate a new version of the polishing stop that improves the planarity of the final layer.

Fabrication of the polishing stop

A 1 mm thick KY(WO₄)₂ sample (Altechna) with a surface area of 10 mm by 10 mm and beveled edges is flip-chip bonded with epoxy based adhesive (EPO-TEK 353ND) onto a SiO₂ substrate with an array of pillars etched on it. The pillars determine the height of the epoxy bonding layer and ensure its uniformity by applying sufficient bonding force with a gimbed pick-up tool. A moderate curing temperature of 80 °C is used to ensure a good bonding quality while avoiding stress in the KY(WO₄)₂ caused by the coefficient of thermal expansion (CTE) mismatch. The pillars on the SiO₂ substrate are fabricated using standard UV-lithography and fluorine based reactive ion etching. The SiO₂ substrate has a total surface area of 20 mm by 20 mm. A 12 mm by 12 mm pool is filled with pillars with a diameter of 6 μm and a spacing of 500 μm. After bonding the KY(WO₄)₂ sample on top of the pillars, a PECVD SiO₂ layer - with the desired final thickness of the KY(WO₄)₂ waveguide core - is deposited on top of the assembly to act as polishing stop.

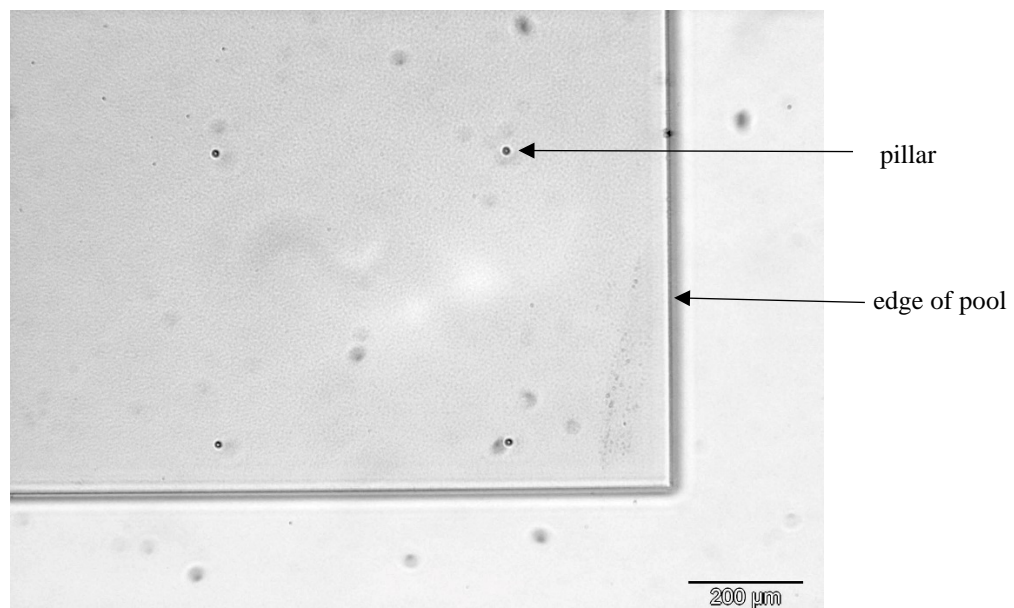


Figure 1: Topview optical microscope image of the pool. Inside the pool, pillars with a diameter of 6 μm and a spacing of 500 μm are clearly visible. The pool is 3 μm in depth.

Thinning procedure

Accurate thickness control is of great importance for high-contrast waveguides. Therefore attention is paid to the planarity of the assembly during the thinning process to get accurate and reproducible layers.

As preparation for the thinning procedure, the assembly of KY(WO₄)₂ sample and SiO₂ substrate is fixed on an ultra-parallel glass plate with a soft quartz wax (Alcowax, Nikka Seiko, JP) with a high degree of planarity. This plate is then positioned inside the

polishing jig and held in place by vacuum. The thinning procedure is performed on a precision lapping and polishing system (Logitech LP50) and consist out of tree stages. First a course lapping step is performed with $9\ \mu\text{m}$ Al_2O_3 particle suspension on an iron disk. During this step the bulk part of the sample, till $\sim 200\ \mu\text{m}$ of thickness, is removed with a removal rate of $\sim 5\ \mu\text{m}/\text{min}$. Coarse lapping is followed by a fine lapping step with $1\ \mu\text{m}$ Al_2O_3 particle suspension on an iron disk. This step is performed till a sample height of $\sim 4\ \mu\text{m}$ above the polishing stop and the removal rate is $\sim 1.5\ \mu\text{m}/\text{min}$. The last step is a combined coarse and fine polishing step. In the first coarse lapping step, $3\ \mu\text{m}$ CeO_2 suspension in combination with $40\ \text{nm}$ SiO_2 suspension are used on a polyurethane disk to remove most of the roughness of the lapping steps with a rate of $\sim 4\ \mu\text{m}/\text{h}$. After approximately 30 minutes the CeO_2 flow is stopped and a fine polish with only the SiO_2 suspension is done till the polishing stop. The removal rate during this final stage is $\sim 1\ \mu\text{m}/\text{h}$ and it reduced to $\sim 200\ \text{nm}/\text{h}$ when it reaches the polishing stop due to the larger surface area.

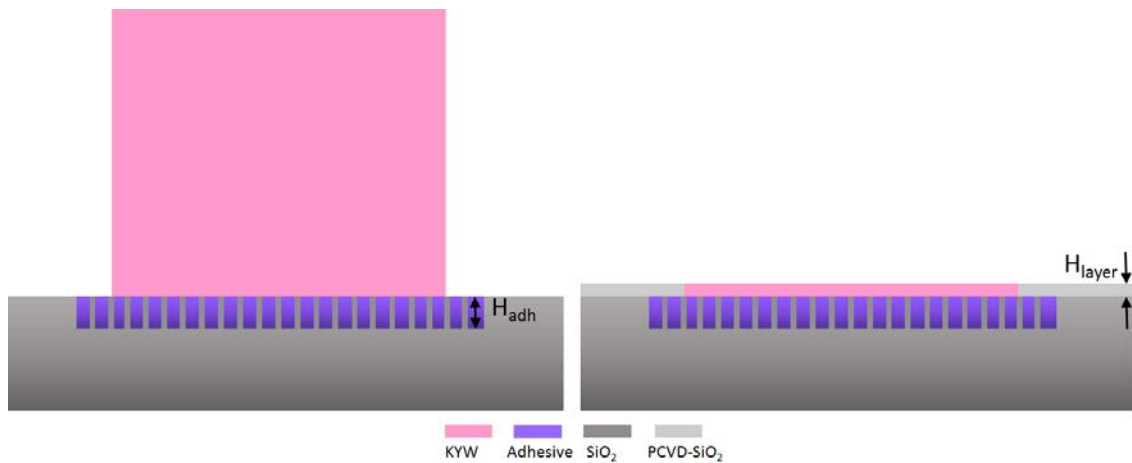


Figure 1: Left) 1mm thick $\text{KY}(\text{WO}_4)_2$ sample flip-chip bonded on a pillar to ensure a fixed adhesive layer. Right) Sample after processing. The PECVD SiO_2 layer reduced the polishing speed to ensure a precise and reproducible layer thickness of the $\text{KY}(\text{WO}_4)_2$.

Results

With this procedure we were able to fabricate a $\text{KY}(\text{WO}_4)_2$ layer with the same thickness as the polishing stop and with acceptable planarity. In future experiments we will improve the planarity of the final $\text{KY}(\text{WO}_4)_2$ layer by using a polishing holder that can adjusted to the planar surface of the SiO_2 substrate.

Conclusion

We have shown the novel fabrication and thinning process of a $\text{KY}(\text{WO}_4)_2$ layer by using a polishing stop to determine the final thickness of the layer and a pillar structure in the substrate to ensure a planar bonding layer. With those additions we are able to fabricate a $\text{KY}(\text{WO}_4)_2$ layer with the same thickness as the polishing stop and with acceptable planarity.

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