

# Adhesive Wafer Bonding of 2 Inch InP to 3 Inch Silicon Wafers for a Membrane Integrated Photonics Platform

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*In this work we present a technique of wafer scale bonding of photonic integrated circuits to a silicon carrier, which enables flexible design of active and passive photonic integrated devices. Exploiting this bonding technique we can use double side processing of the photonic membrane, avoid planarization steps and achieve high index contrast in the waveguides, which supports the design of complex systems with small footprint.*

## Introduction

Photonic integration on membranes is a promising solution to heterogeneously combine electronic and photonic functionalities in a single chip. Heterogeneous integration in silicon on insulator (SOI) has shown several devices for datacom applications [1], [2]. Also, III-V membrane technology using a multi regrowth approach [3] has been exploited, aiming for on-chip interconnection. The InP membrane on Silicon (IMOS) platform [4] is an advantageous solution for both applications since it can integrate all the active and passive building blocks, such as lasers, detectors and high-index-contrast waveguide devices, in a single membrane layer. The high index contrast allows us to have all the passive waveguide components with dimensions of 400 nm width and 300 nm height. The schematic of IMOS platform is shown in Fig. 1.a.

The platform has all the important building blocks to create complex systems. Previously in the IMOS platform we realized building blocks such as high gain semiconductor optical amplifiers (SOA) [5] (see Fig. 1.b and 1.c), tunable ring resonators [6], variety of passive components [4] and simple laser circuits based on those building blocks [7], [8]. In the next chapter we will give more details on the fabrication process and, in particular, on the adhesive wafer bonding technique used for the fabrication of the membrane photonic integrated circuits.

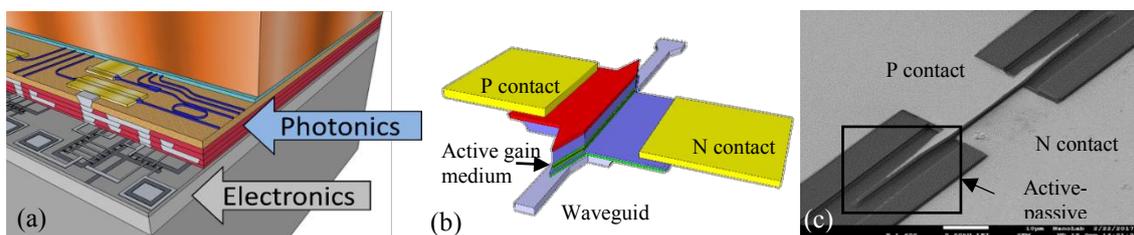


Fig. 1. (a) The schematic of IMOS platform; (b) The schematic of the SOA building block; (c) SEM image of the fabricated SOA.

## Fabrication process and wafer bonding

To achieve high index contrast we use photonic membrane layer where we include all active and passive devices (see Fig. 2.a). To support the membrane we use a silicon carrier which can also carry the electronics and driving circuits for our membrane photonic integrated circuits (see Fig. 2.b). We exploit the double side processing approach to achieve much flexible fabrication and design of the devices [9]. This approach helps us to avoid planarization steps, which are always difficult to control. We use adhesive wafer bonding technique to bring two wafers into the physical contact.

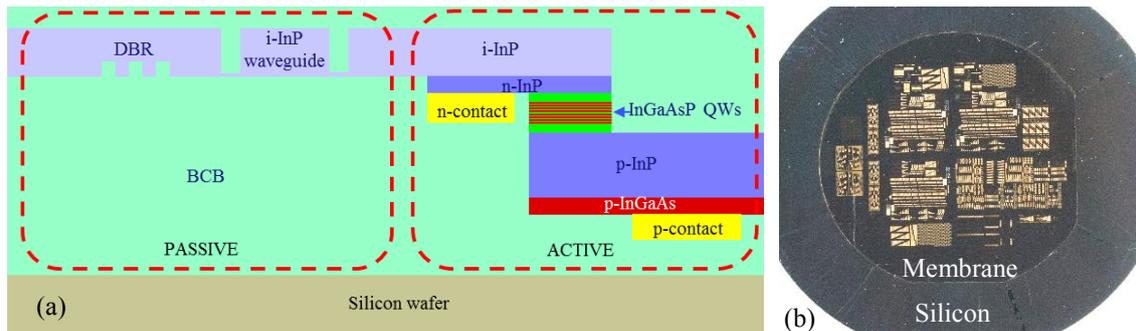


Fig. 2. a) Schematic of the integration on the membrane platform. b) photograph of the fabricated wafer with a variety of circuits and devices.

The fabrication process of the platform uses double side approach and can be divided on two large blocks. The first block is the processing of InP wafer before bonding to the silicon. The second block includes bonding procedure and post processing on the other side of the membrane. The processing starts with the MOCVD growth of epitaxial layers of active-passive stack. The schematic of the fabrication process is shown in Figure 3.

The first step to do is to define deep etched markers for optical and electron beam lithography. Secondly, we etch left side of the mesa according to Fig. 8.a. After that we remove lossy n-doped material from the top of the intrinsic wave guiding layer. Then we deposit two metal layers for n and p ohmic contacts. After these steps are done we can continue with bonding process of 2 inch InP wafer to 3 inch silicon carrier wafer.

The process flow of the bonding consists of the following steps. We deposit a thin layer of silicon dioxide on both the silicon and InP wafers for better adhesion of the polymer. Then we spin BCB polymer on the InP wafer, which has been patterned and contains topology of 1.5  $\mu\text{m}$  step height. Then we bring the two wafers into contact in a dedicated wafer aligner and bond them under vacuum, high force and a temperature of 280  $^{\circ}\text{C}$ .

After bonding is done we remove the backside of the InP wafer in concentrated hydrochloric acid and continue our processing on the other side of the membrane. Firstly, we define shallow etched grating structures while surface is flat and clean. After that we etch waveguides together with right side of the mesa and photonic crystal structures, which gives us perfect alignment of those three features. After all the definition of the devices are done we perform the access to the metal contact which is under the membrane at this stage. We do wet etching of the membrane to access those contacts. After that we perform several lithographies to create the metallic heat sink to the silicon wafer together with general metal wiring and heating structures over the wafer. For that we etch the BCB bonding polymer next to the metal contact using metal as an etching mask. Then we spin polyimide layer to create optical buffer for heaters and wiring. Then we reflow the

polyimide to create the slope for the metal and perform lift-off lithography to deposit heat sink and wiring structures on our wafer.

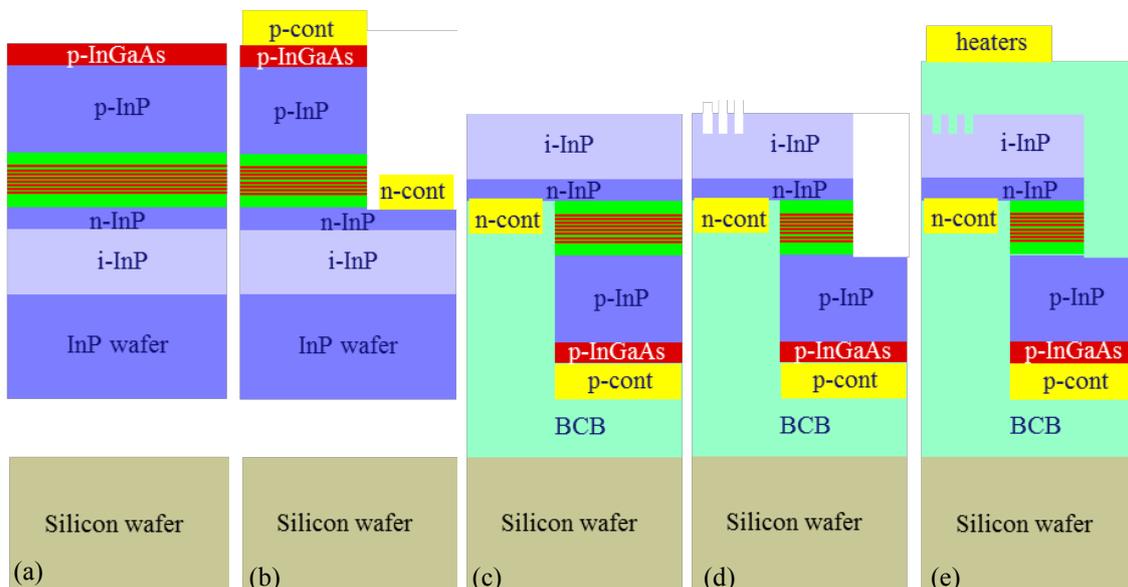


Fig. 3. Schematic of the fabrication process of the IMOS platform. a) Epitaxial layers grown in InP wafer; b) pre bonding processing of the InP wafer; c) bonding and substrate removal; d) post bonding semiconductor processing in InP; e) heaters and heat sink definition.

## Conclusion

Wafer scale bonding technique allows highly flexible membrane photonic integrated circuits. We demonstrated a double sided fabricated wafer based on the adhesive bonding technique. The wafer contains more than 10 unique designs from different users. These designs include both passive and active devices, among them also SOAs [5] and DBR-lasers [7], [8].

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